

# Design of a Low-Power CMOS LVDS I/O Interface Circuit

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**Abstract:** The paper presents the design and implementation of LVDS (low-voltage differential signaling) receiver circuit, fully compatible with LVDS standard. The proposed circuit is composed of the telescopic amplifier and the comparator with internal hysteresis. The receiver supports 3.5 Gbps data rate with 7.4 mA current at 1.8 V supply according to post-layout circuit simulations. The circuit has the power consumption of 13.1 MW. Comparing with the conventional circuit, the circuit is achieved to reduce the power consumption by 19.1% and the data rate by 14.3%. The validity and effectiveness of the proposed circuit are verified through the circuit simulation with Samsung 0.18  $\mu\text{m}$  CMOS (complementary metal-oxide-semiconductor) standard technology under the 1.8 V supply voltage.

**Key words:** Low-power circuit, LVDS, interface circuit, CMOS high-speed circuit, telescopic amplifier.

## 1. Introduction

The ever increasing processing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc., is pushing the off-chip data rate into the gigabits-per-second range. However, unlike internal clocks, chip-to-board signaling gains little benefit in terms of operating frequency from the increased silicon integration. While the reduction of the power consumption is the great concern in battery-powered portable systems, it is also required in other systems to reduce the costs related to packaging and additional cooling systems. Many developments in high speed serial I/O (input/output) are pushing the off-chip data rate into multi-Gbps range on a single pin/wire. Along with the increasing data rate, other major concerns of high performance I/Os are reductions in circuit power and chip area, which enable very high levels of silicon integration [1]. One of the effective solutions to multi-giga-bit transmission is LVDS (low-voltage differential signaling) which possesses significant advantages such as fast data rate and good energy efficiency by means of reducing

signal swing on the wire [2-4]. Defined in LVDS standards specification, it is the most common differential interface [4-7]. The standard only specifies the electrical characteristics of drivers and receiver suitable for LVDS applications. It is, therefore, an electrical-only standard, commonly referred to by higher level protocol standards as their interface or physical layer [8].

This paper presents the design and implementation of the LVDS receiver circuit using 0.18  $\mu\text{m}$  CMOS (complementary metal-oxide-semiconductor) standard technology under the 1.8 V supply voltage. The proposed circuit is composed of the telescopic amplifier and the comparator with internal hysteresis. The receiver circuit supports transmission at data rates of 3.5 Gbps and exhibits average currents of 7.4 mA with circuit simulation. This paper is organized as follows: Section 2 discusses the LVDS link and LVDS drivers. In Section 3, the typical LVDS receiver and proposed LVDS receiver are discussed. In Section 4, Experimental result and physical design are presented. Finally, we make conclusions in Section 5.

## 2. LVDS Link

The LVDS link block diagram, as shown in Fig. 1,

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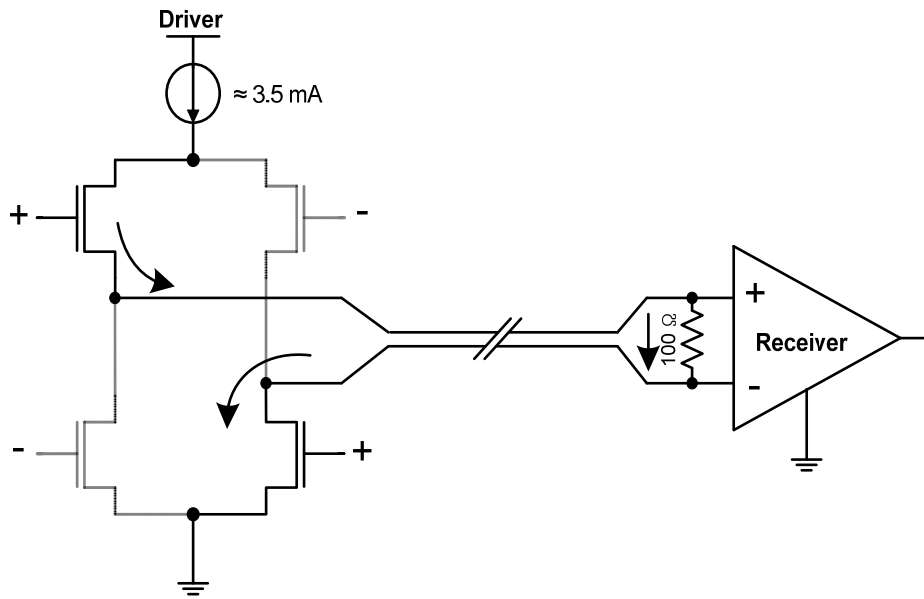


Fig. 1 Simplified LVDS link block diagram.

shows an equivalent diagram of the driver and the receiver. The driver tends to be a current-mode driver, driving the balance interconnect cable to a load consisting of the termination resistor and the receiver. The current is steered down through the resistor and for the other, the direction of the current is reversed up through the resistor. The proper levels will not be obtained without the resistor in place as it completes the current loop. It is also needed to provide termination due to the fast edge rates. The current source driver minimizes switching spikes in the driver output structure. The receiver input is high impedance so that the majority of the current flows through the termination resistor and returns to the driver. This is known as odd-mode transmission. The odd-mode transmission is not only an EMI (electromagnetic interface) advantage, but also makes the signal path more tolerant to imperfections in the ground plane, thus another advantage.

The LVDS interface driver, as shown in Fig. 2, has a low-voltage swing, it is connected to point-to-point and is achieved to very high data rates and is reduced by the power dissipation [1]. The LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. A differential load

resistor at the receiver end provides optimum line impedance matching. Due to the imperfect termination, package parasitic, component tolerances or crosstalk, there are reflected waveforms returning to the driver. The LVDS is a standardized data transmission format that is widely used for serial data transmissions, a differential signal is centered at a common mode voltage of about 1.25 V. The maximum magnitude of the differential signal is 300 mV. Typically, the LVDS signal is varied in magnitude from 1.1 V to 1.4 V.

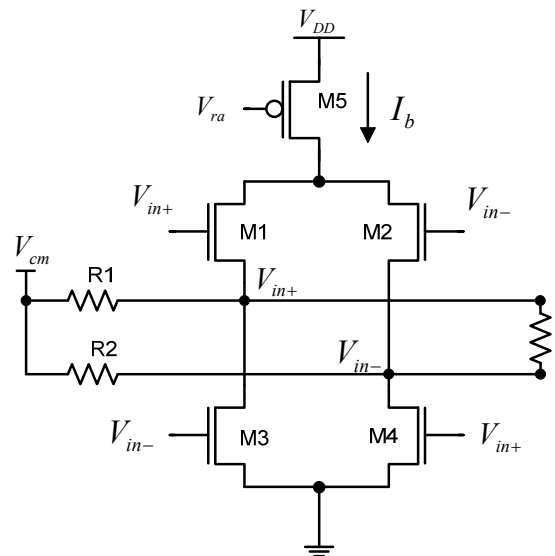


Fig. 2 Typical LVDS driver.

A typical bridged-switched LVDS driver behaves as a current source with switched polarity. The bias current  $I_b$  is switched through the termination resistors according to the data input, and thus produces the correct differential output signal swing. It uses four transistor switches (M1-M4) in a bridged configuration. If switches M1 and M4 are on ( $V_{in} = \text{HIGH}$ ), the polarity of the output current is positive together with the differential output voltage. On the contrary, if switches M1 and M4 are off (switches M2 and M3 are on), the polarity of the output current and voltage is reversed. With a nominal  $100 \Omega$  load at the receiver, both the common mode voltage and the differential swing at the output should fall within the LVDS standard specifications over the full range of process, supply voltage 3.3 V, and temperature variations,  $25^\circ\text{C}$  PVT (process-voltage-temperature) where  $V_{OD}$  and  $V_{CM}$  are the differential output voltage and the common mode voltage at the transmitter output, respectively.

The LVDS driver stage operates with a 3.5 mA (typical) current source that is always on. The logic ones and zeros on the bus are created by simply rerouting the current in different directions through the conductors of the differential pair. It is this always-on characteristic that eliminates switching noise and EMI. Designed for point-to-point signal transmission, the LVDS utilizes a simple termination scheme. A single 100-ohm resistor placed at the receiver input terminates the differential pair, thus eliminating reflections. Because of the high-impedance receiver input, the entire current of the driver's current source flows through the termination resistor generating a low, differential bus voltage of 250 mV nominal. This voltage swings around a 1.2 V common-mode potential, which is the typical driver output offset voltage. The LVDS standards define stringent specifications on the signal swings and signal levels. For off-chip I/O, the LVDS standards define the swing and common mode voltage as:

$$250 \text{ mV} \leq V_{OD} \leq 350 \text{ mV} \quad (1)$$

$$1.125 \text{ V} \leq V_{CM} \leq 1.375 \text{ V} \quad (2)$$

where,  $V_{OD}$  and  $V_{CM}$  are the differential-mode output voltage and common-mode output voltage at the driver output, respectively. Also, the LVDS standards define LVDS levels of the receiver as:

$$|V_{DMIN}| \geq 100 \text{ mV} \quad (3)$$

$$100 \text{ mV} \leq V_{CMIN} \leq 2.4 \text{ V} \quad (4)$$

where,  $V_{DMIN}$  and  $V_{CMIN}$  are the differential-mode input voltage and common-mode input voltage at the receiver end, respectively.

### 3. Proposed LVDS Receiver

The operation speed of the LVDS is more sensitive to the receiver than the driver [6]. To enhance the LVDS performance, it is essential to design the high speed and low power LVDS receiver. General LVDS receiver preamplifier is composed of latch type sense amplifier, as shown in Fig. 3. Receiver preamplifier acts role that send amplifying small input signal that enter with high speed. Latch type sense amplifier has

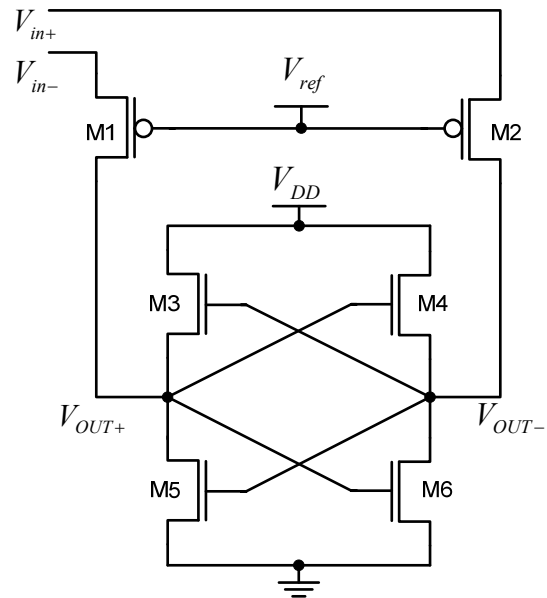


Fig. 3 Typical latch type sense amplifier.

higher transmission speed more than existent differential amplifier type sense amplifier. Transistor M1, M2 is connected to act sense amplifier stable in current mode.  $V_{ref}$  can control bulk of amplification. If amplification degree has great regulating,  $V_{ref}$  have trade-off relation that the delay grows. The receiver preamplifier with the latch type sense amplifier has the output swing of 0.42 V.

Fig. 4 shows the block diagram of the proposed LVDS receiver. The proposed receiver circuit is composed of the telescopic amplifier, the comparator with internal hysteresis, and reference bias unit. Fig. 5 shows the telescopic amplifier. All transistors are biased in the saturation region. Transistors M1 and M2, M7 and M8, and the tail current source M9 must have at least  $V_{ds, sat}$  to offer good common-mode rejection, frequency response and gain. The maximum differential output swing of a telescopic op-amp is shown to be  $2V_{sup}-10V_{ds, sat}-6V_{margin}$ .

At large supply voltages, the telescopic architecture becomes the natural choice for systems requiring moderate gain from the op-amp. Reducing supply voltages, on the other hand, forces reconsideration in favor of the folded cascode, or, in the extreme case, the two-stage design. Although a telescopic op-amp without the tail current source improves the differential swing by (600 mV), the common-mode rejection and power-supply rejection of such a circuit is greatly compromised. Moreover, the performance parameters, such as unity-gain frequency and settling time of an op-amp with no tail or with a tail transistor in the linear

region is sensitive to input common-mode and supply-voltage variation, which is undesirable in most analog systems. The telescopic amplifier has higher frequency capability and consumes less power dissipation than other topologies. In this work, we set the bias current 80  $\mu$ A for adequate margin and different  $V_{DS}$  in the reference generator and tail current source. To do so, we set the width-to-length ratio (W/L) of transistor M9,  $(W/L)_{M9}$ , to 60. Taking half the tail current, we set the aspect ratio of transistors M7 and M8,  $(W/L)_{M7, 8}$ , to 30, respectively. For high compliance current mirror and bias voltage, two transistors, M5 and M6, are identical. We set the aspect ratio of transistors M5 and M6,  $(W/L)_{M5, 8}$ , to 6.6, respectively. To cascode current mirror stage where there are four PMOS transistors, which are identical, and the current passing through all of them is same as that of the previous stage. We set the aspect ratio of transistors M1, M2, M3 and M4,  $(W/L)_{M1, 2, 3, 4}$ , to 1, respectively.

Fig. 6 shows the comparator with internal hysteresis. To enhance the performance of the LVDS, we adopt the telescopic amplifier and comparator with internal hysteresis in the LVDS receiver. The positive feedback of the circuit gives the hysteresis and reduces the propagation delay time. The comparator has the hysteresis voltage of 72 mV and the propagation delay time of 1.21 ns.

#### 4. Experimental Result and Physical Design

All simulations are carried out with HSPICE using

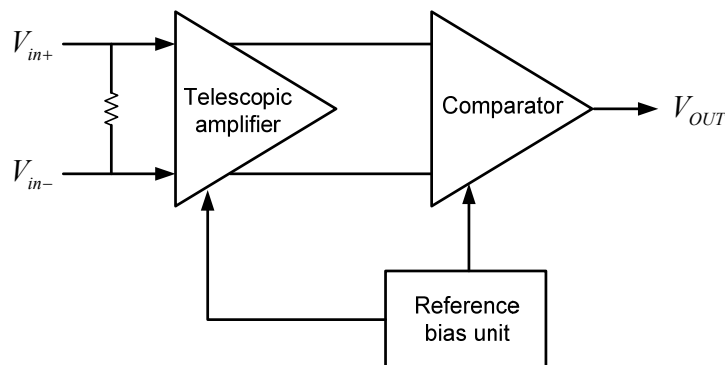


Fig. 4 Block diagram of receiver.

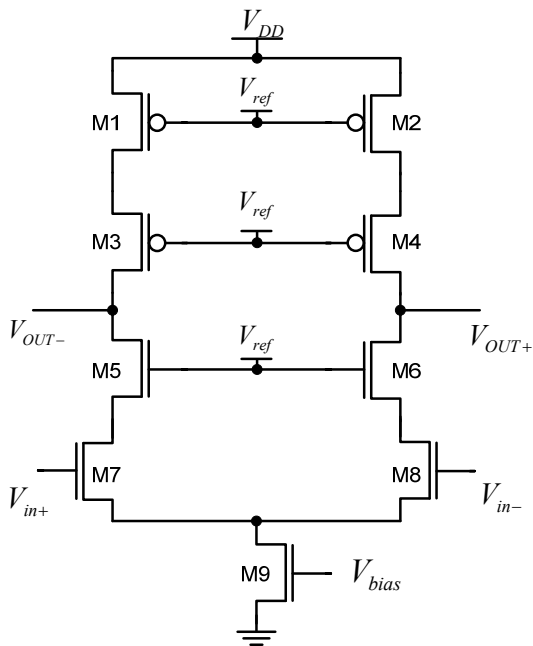


Fig. 5 Telescopic amplifier.

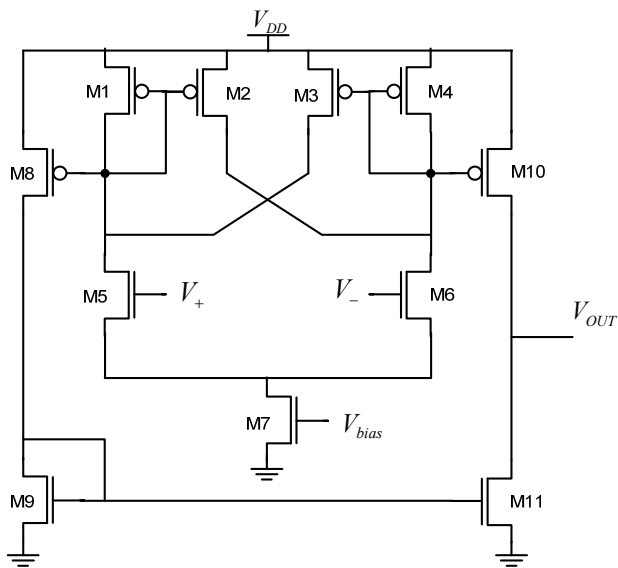


Fig. 6 Comparator with internal hysteresis.

Samsung 0.18  $\mu\text{m}$  CMOS technology under the 1.8 V supply voltage. Fig. 7 shows the layout of proposed LVDS receiver.

Table 1 shows comparison results of sense amplifier and telescope amplifier. The data rate is improved by 16.7% by gain's increase compare to latch type sense amplifier. However, the power consumption is increased by 9.6% than latch type sense amplifier.

Table 2 summarizes the performance comparisons

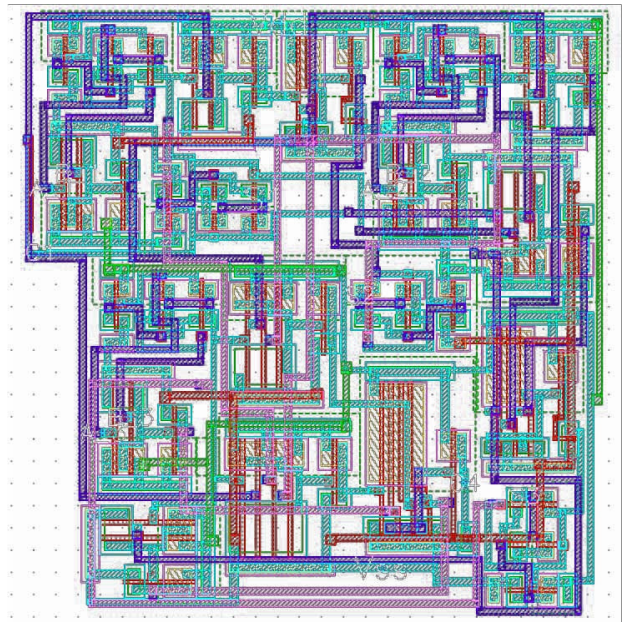


Fig. 7 Layout of LVDS receiver amplifier.

Table 1 Comparison table of sense amplifier and telescopic amplifier.

	Sense amplifier	Telescope amplifier
Gain	Low	High
Output swing	250 mV	250 mV
Data rate	3.0 Gbps	3.5 Gbps
Power consumption	11.5 MW	12.6 MW

Table 2 Comparison table of LVDS receiver.

	Proposed	Previous
Output swing	250 mV	250 mV
Power consumption	13.1 MW	15.6 MW
Current	7.4 mA	8.6 mA
Data rate	3.5 Gbps	4 Gbps

on the data rate and power consumption between the proposed receiver and the previous works. Compared with the previous work, the proposed circuit is achieved by power reduction of 19.1%. However, the circuit has the decrease in data rate of 14.3%.

## 5. Conclusions

This paper describes the LVDS receiver circuit using telescope amplifier and comparator with internal hysteresis. The limits of the typical LVDS receiver were overcome by the telescopic amplifier architecture featuring a maximum transmission speed of 2.5 Gbps. The proposed LVDS receiver modified closed loop

switching current circuit to maintain reliable signal current levels and controlled common-mode voltage levels with a reduced output swing. The receiver uses telescope amplifiers and out-buffer with feedback to achieve optimized gain performance for low differential input swing, while reducing power consumption. The receiver supports 3.5 Gbps data rate with 7.4 mA current at 0.18  $\mu\text{m}$  CMOS standard technology under the 1.8 V supply voltage. Future work is the circuit design to achieve the higher data rate.

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