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Impacts of Parameter Scaling for Low-Power Applications Using CNTFET (Carbon Nanotube Field Effect Transistor) Models: A Comparative Assessment

Atheer Al-Shaggah[1], Abdoul Rjoub[2] and Mohammed Khasawneh[1]

1. Electrical Engineering Department, Jordan University of Science and Technology, Irbid 22110, Jordan

2. Computer Engineering Department, Jordan University of Science and Technology, Irbid 22110, Jordan

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Abstract: This paper provides an extension to the earlier work wherein a comparison between different models that had studied the effects of several parameters scaling on the performance of carbon nano tube field-effect transistors was presented. The evaluation for the studied models, with regard to the scaling effects, was to determine those which best reflect the very essence of carbon nano-tube technologies. Whereas the models subject this comparison (Fettoy, Roy, Stanford, and Southampton) were affected to varying degrees due to such parametric variations, the Stanford model was shown as still being valid for a wide range of chiralities and diameter sizes; a model that is also applicable for circuit simulations. In this paper, we present a comparative assessment of the various models subject to the study with regard to the effect of incorporating multiple carbon nanotubes in the channel region. We also assess the effect of oxide thickness on transistor performance in terms of the supply voltage threshold effects. Results leveraging our findings in this ongoing research endeavor reveal that many research efforts were not efficient to high degree due to high delay and not valid for circuit simulations.

Key words: Ballistic effects, CNT (carbon nanotubes), CNFET (carbon nanotube field-effect transistor), energy-saving technologies, low-power applications, compact modeling, SPICE simulations.

1. Introduction

The process of component size shrinkage is rather vital as components become packed more densely than ever before [2]. Several challenges present themselves in various ways, with current leakage being the most influential since it dissipates energy, confuses nearby transistors and distorts electric signals [3]. CNTFET (carbon nano tube field effect) transistors have been recently shown to reflect better performance than traditional silicon MOSFETs (metal oxide semiconductor field effect transistor) [4], since CNTFET inherently circumvents the limitations of scaling MOSFETs less than 22 nm according to ITRS (International Technology Roadmap for Semiconductors) [5]. This is due to the fact that CNT exhibit promising mechanical and electrical properties; including high mobility which reflects in improved conductivity, which when involved in transistor structures it reflects in excellent performance with high ON/OFF current ratio and low inverse subthreshold swing [6].

There are two types of CNTFETs that are different in their current injection methods: The first type is ballistic CNTFETs where the source and drain are doped due to the presence of Ohmic contacts with the channel being intrinsic. This type has higher "ON" current and exhibits high performance near ideal sub-threshold slope. The second type is the Schottky Barrier CNTFET with metal source and drain where

Corresponding author: Atheer Al-Shaggah, master student, research fields: modeling and simulation of CNTFET. E-mail: atheer.m.sh@gmail.com.

tunneling of electrons and holes at source and drain junctions from the potential barrier is governed by transport through the channel [7, 8].

For ballistic CNTFETs, big efforts were made recently to introduce a complete simple model describing performance and electrical behavior of CNTFETs in circuits as a successful alternative to the conventional transistor with regard to several parameters that pose an impact on its performance [9]. The concept of CNTFET is still fairly recent where it depends on numerical models that require large number of iterations for convergence. In recent years, ongoing research endeavors have revealed a number of CNTFET computer models that are compatible with SPICE that helps a great deal in evaluating delays, estimating power requirements and simulating any performance degradation. Further, it makes multiple transistor circuit simulations more viable [10-15].

Various models were introduced to simulate current voltage characteristics of CNTFETs. Most of these were derived according to the statistical physics of CNT with the inclusion of quantum mechanical effects such as mobile charge density. In addition, some of these models were derived using approximations like piecewise linearization to minimize the computational complexity. Other models use the direct solution and closed forms with smooth functions for the same reason.

In this paper, different models for ballistic CNTFET current voltage characteristics [1] will be investigated, analyzed and compared. The comparison between these models includes: direct effects of channel length (L_g) scaling on CNTFET performance with semiconducting CNT by using different channel lengths L_g for the same CNT. Moreover, the impact of the supply voltage on CNTFET performance, and the dioxide thickness impact on its performance will be investigated. Further, the impact of the number of CNTs used in the channel region on the current voltage characteristics of the CNTFET will be studied. Hence, this paper focuses primarily on the structure of a "MOSFET-like CNTFET", where the structure of a CNTFET is inherently very similar to conventional MOSFETs [7, 16].

The rest of the paper is organized as follows: Section 2 presents theory of CNTFET; several models will be analyzed and discussed in Section 3. Simulations and results are presented in Section 4. Finally, Section 5 is allotted to conclusions based on the work presented in this paper.

2. Theory of CNTFET

A CNT (carbon nano tube) is a graphene sheet wrapped around to a cylindrical nanostructure, which would constitute the core of a CNTFET as it acts as a semiconducting channel [17]. A SWCNT (single-walled CNT) can either be a conductor or semiconductor depending on the chirality vector that is represented by an ordered pair of integers (n, m) [16]. A simple method to determine if a CNT is metallic or semiconductor-like is determined from its indexes (n, m); to that end, a nanotube is metallic if $n = m$ or $n - m = 3i$, where i is an integer. Otherwise, the tube is a semiconductor [18]. The diameter of the CNT can be calculated based on the following:

$$D_{CNT} = \frac{\sqrt{3}\,a_0}{\pi}\sqrt{n^2 + nm + m^2} \tag{1}$$

where a_o = 0.142 nm is the inter-atomic distance between a carbon atom and its immediate neighbor. The diameter of a CNT has a direct impact on the threshold voltage, where it can be approximated to first order as half the band gap energy that is an inverse function of the diameter as follows:

$$V_{th} \cong \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a\,V_\pi}{e\,D_{CNT}} \tag{2}$$

where, a = 2.49 A is the carbon-to-carbon atom distance, V_π = 3.033 eV is the carbon π-π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter.

A typical device structure for a MOSFET-like CNTFET is shown in Fig. 1, where it has four terminals just like a conventional silicon device. Hence, ballistic CNTFET is more appropriate for MOSFET-like CNTs;

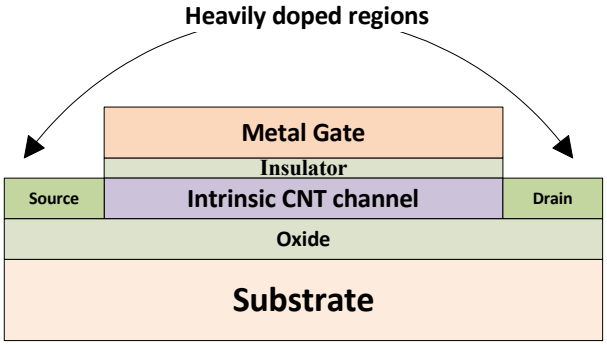

Fig. 1 Schematic diagram of a carbon nanotube transistor: cross sectional.

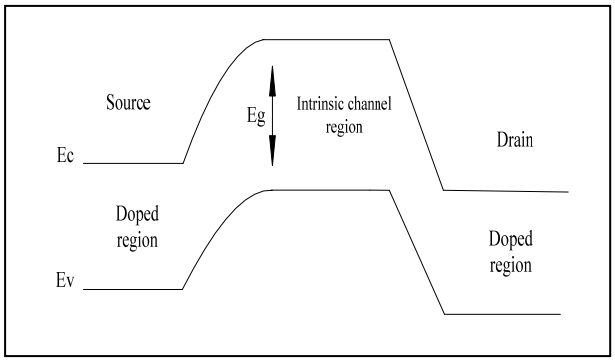

Fig. 2 Energy band diagram for channel region of CNTFET.

ballistic CNTFET has undoped intrinsic channel region with the other regions being heavily doped. The source and drain act as extension regions or interconnects between two adjacent devices [19]. The electronic transport for such transistor is ballistic where the Fermi level profile and the energy band diagram in the channel region are shown in Fig. 2 [7].

3. Model Analysis

Over the past decade, various models investigated the current voltage characteristics, performance of CNTFET and its application in circuit design. One example would be the CNTFET Fettoy Simulator. This simulator analyzes the ballistic current voltage characteristics for a carbon nano tube MOSFETs to high accuracy. Only the lowest subband is considered, but it is readily modifiable to include multi sub-bands [10, 11]. Although this tool is only valid for a single transistor it is still the base for other CNTFET models. It depends primarily on deriving the surface potential (φ_s) by decomposing it into two voltages: a Laplace potential V_L and a potential V_P due to mobile charge as follows:

$$\varphi_s = V_L + V_P \quad (3)$$

In Ref. [12], meanwhile, a model which depends mainly on Fettoy simulator is presented. Therein, the work presents a novel surface potential based on SPICE (simulation program with integrated circuit emphasis) compatible modeling techniques using a polynomial approach for fitting the parameters in order to improve the runtime significantly. This model enables delay evaluations, power estimation, and simulates performance degradation due to interconnect and parasitic components. It, also, is applicable for a wide range of diameters ranging from 0.6 nm to 3.5 nm and accounts for all chiralities as long as they are semiconducting. Nonetheless, the performance of CNTFET, according to the model, stands incoherent against varying device parameters. Furthermore, the model is not valid for all operating regions, as shown in Fig. 3.

On the other hand, the Stanford Model is a complete circuit-compatible compact model for single-walled (CNTFETs). With its inception, it was the first time to have a universal circuit-compatible CNTFET model, implemented in HSPICE, accounting for practical device nonidealities, which included elastic scattering effects in the channel region, resistive S/D (source/drain) regions, the Schottky-barrier resistance, and the parasitic gate capacitances.

In its derivation, a sum in lieu of an integral was used as presented in Ref. [13]. Under this formulation more than just one nanotube per device can be modeled. The current voltage characteristics pursuant with the Stanford model are shown in Fig. 4.

The Southampton Model, on the other hand, is a more recent model that incorporates ballistic as well as non-ballistic transport effects. This model is based on cubic spline approximation of non-equilibrium mobile charge density, where approximations were made to solve for the self-consistent voltage originally defined as a non-linear function of terminal capacitance

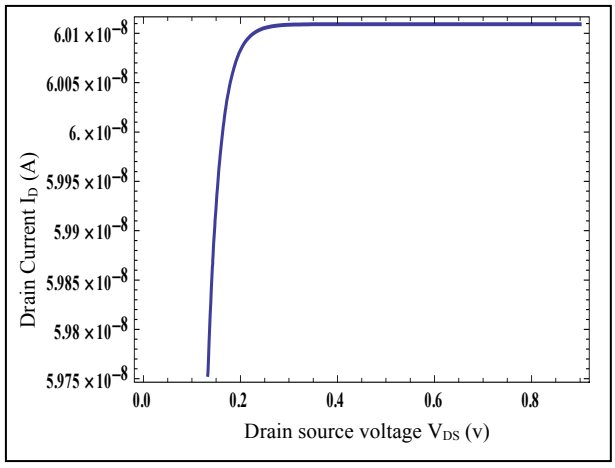

Fig. 3 Current voltage characteristics for Ref. [12]: I_{DS} vs. V_{DS} at V_{gs} = 0.9 V.

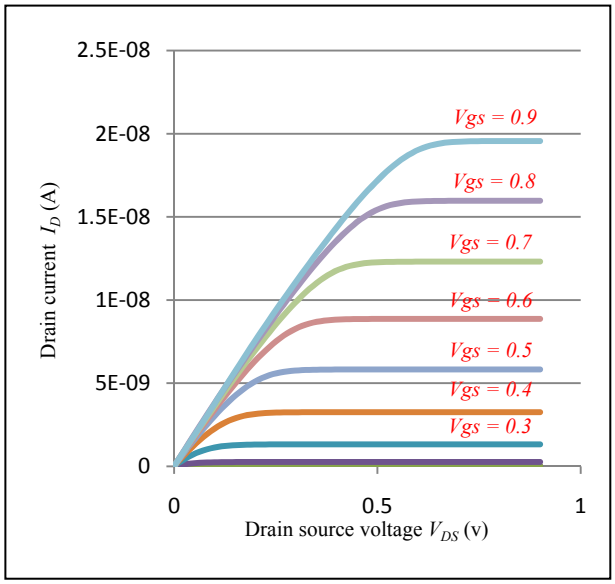

Fig. 4 Stanford model current voltage characteristics: I_{DS} vs. V_{DS} for chirality (19, 0), different V_{gs} (V) and T = 300 K.

reducing the cost of the number of Newton-Raphson iterations needed [14]. Consequently, the model was developed to get around the main stumbling block in circuit-compatible modeling for CNTFETs, supplemented by the fact that accurate calculations for mobile charges inherently involve numerical integration of the DOS (density of states) given by Eqs. (4) and (5) over the number of allowed energy levels using a Fermi probability distribution [15].

$$N_S = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)\ f(E - U_{SF})\,\mathrm{d}E \quad (4)$$

$$N_D = \frac{1}{2}\int_{-\infty}^{+\infty} D(E)\ f(E - U_{DF})\,\mathrm{d}E \quad (5)$$

where, N_S is the density of positive velocity states filled by the source and N_D is the density of negative velocity states filled by the drain. Here, the self-consistent voltage is related to the terminal voltages and charges at terminal capacitances through a nonlinear algebraic formula described by the following mathematical formulation [14]:

$$V_{SC} = \frac{-Q_t + qN_S(V_{SC}) + qN_D(V_{SC}) - qN_0}{C_{tot}} \quad (6)$$

where, Q_t is the charge stored in the terminal capacitances, C_{tot} is the total terminal capacitance and N_o is the equilibrium electron density. Hence, according to the ballistic transport theory [20], the drain current crossing the nanotube using the Fermi-Dirac integral with order zero is given by:

$$I_{ds} = \frac{2qkT}{\pi h'}\left[F_0\left(\frac{U_{SF}}{kT}\right) - F_0\left(\frac{U_{DF}}{kT}\right)\right] \quad (7)$$

Now, once the value of the self-consistent voltage is known from the energy difference of Fermi levels and the self-consistent voltage for both source and drain, U_{SF}, U_{DF}, respectively, the drain current can be readily found as shown in Fig. 5.

4. Simulations and Results

Scaling has a rather significant effect on the electrical behavior of a transistor. There are several parameters that bear a pronounced effect on the performance of a CNTFET. This includes, amongst others, length of channel; normally referred to as short channel effect. Recent research efforts show that this effect has been investigated for CNTFETs [21]. Also, supply voltage proves to be very important since it has significant bearing on the power dissipation of a transistor. Other parameters include oxide thickness that has direct bearing on tunneling current.

Results of simulations show that all models are affected by scaling to varying degrees, starting with the Stanford model which is impacted significantly due to the amount of channel scaling as shown in Fig. 6. From results in the figure, it is obvious that "ON" and "OFF" currents are decreased by decreasing L_g, however, at a

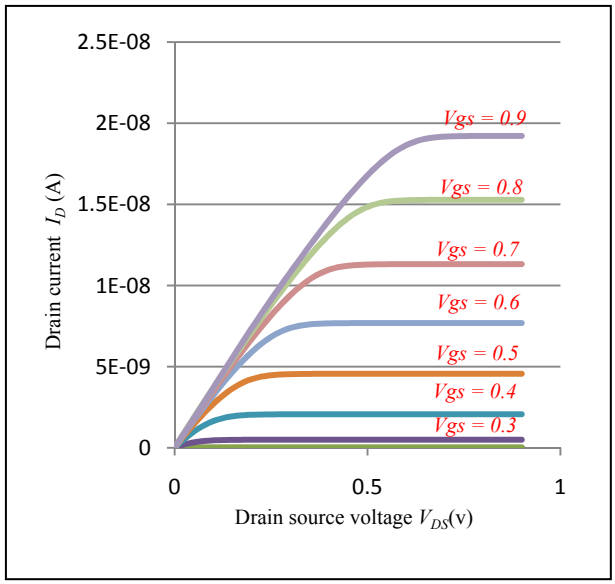

Fig. 5 Current voltage characteristics for Southampton model for chirality (19, 0), at different V_{gs} (V) and T = 300 K.

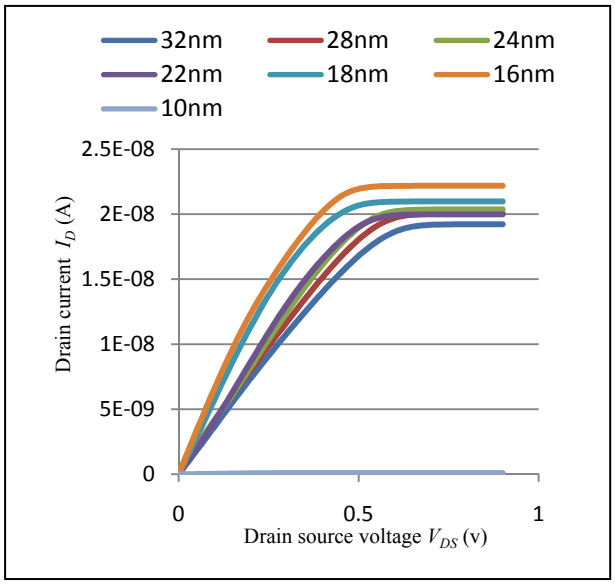

Fig. 7 Scaling effect on Southampton model at different channel lengths at V_{gs} = 0.9 V.

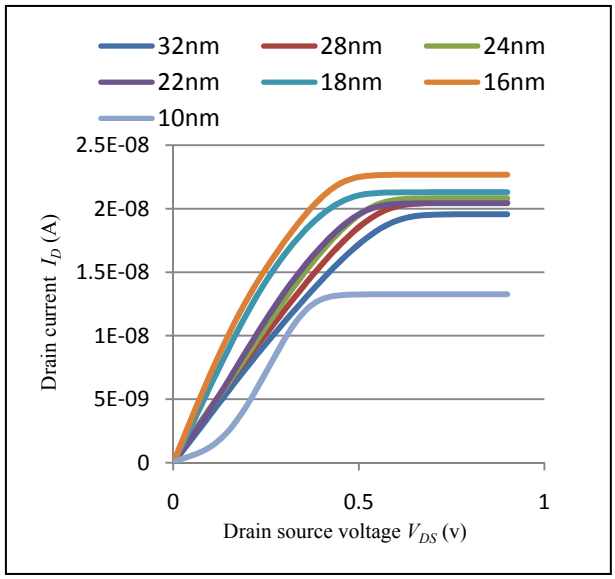

Fig. 6 Scaling effect on Stanford model at different channel lengths at V_{gs} = 0.9 V.

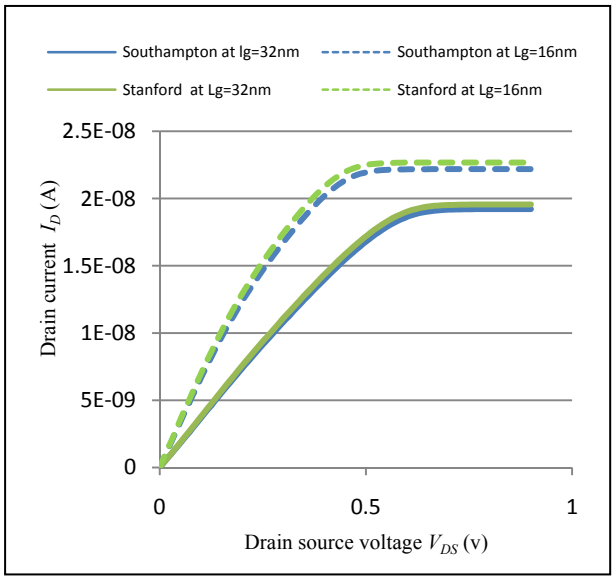

Fig. 8 Comparison of current voltage characteristics between both models at 16 nm and 32 nm channel length.

significant increase in the ON/OFF ratio, with similar results evident for the Southampton model from Fig. 7. Upon comparing the two models, the Southampton model shows better performance due to scaling the length of the channel as manifested in Fig. 8.

It is worthy of noting, however, that at 10 nm channel length model simulations reveal huge differences between Southampton and Stanford models as illustrated in Fig. 9. These differences, at very small scales, come about as a result of various quantum mechanical effects.

On the other hand, oxide thickness has an impact on a CNTFET where it is evident for all models since thinner oxide thickness gives rise to more current and consequently electrons will pass easily across the channel. This is quite evident by examining model simulations in Figs. 10-12 for Fettoy, Stanford and Southampton models, respectively. In these figures we show drain current as a function of oxide thickness where the supply voltage V_{DD} plays out as varying parameter. These simulations were based on a CNT

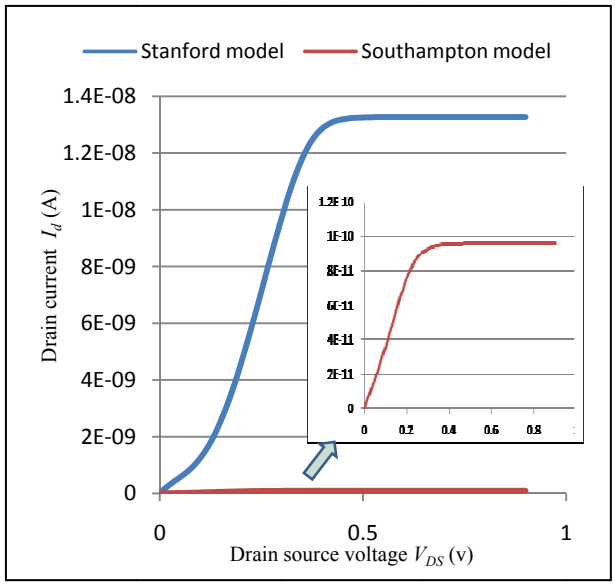

Fig. 9 Mparison between both models current voltage characteristics at channel length L_g = 10 nm.

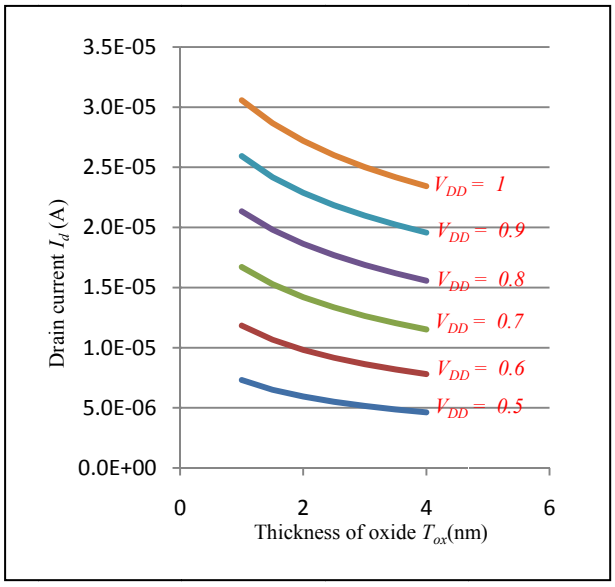

Fig. 10 Fettoy tool current behaviour for different supply voltages V_{DD} (V) as function of oxide thickness T_{ox}(nm).

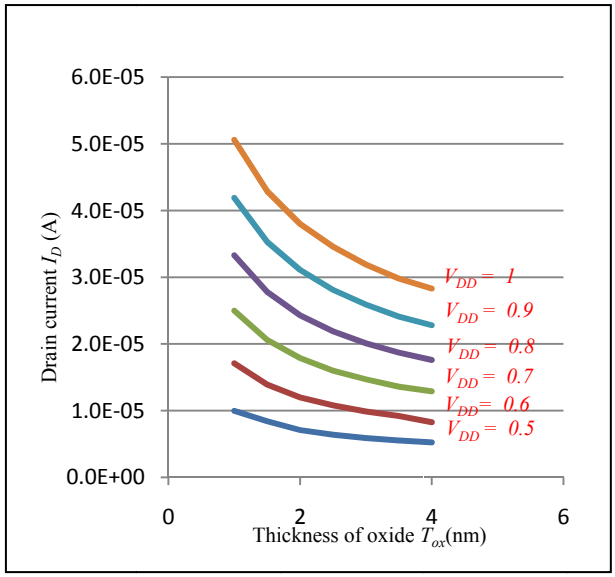

Fig. 11 Tanford model current behaviour for different supply voltages V_{DD}(v) as function of oxide thickness T_{ox}(nm).

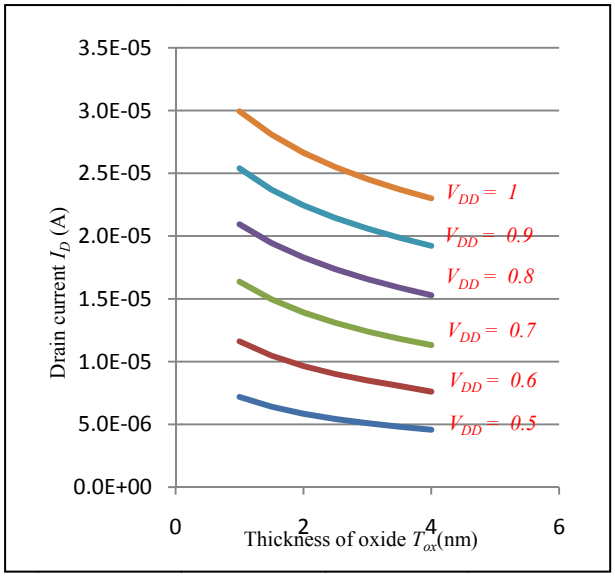

Fig. 12 Outhampton model current behaviourfor different supply voltages V_{DD}(v) as function of oxide thickness T_{ox}(nm).

with chirality (19, 0), at diameter d = 1.49 nm, with threshold voltage V_{th} = 0.293 V, and a temperature of T = 300 K. Based on these results (Figs. 10-12), it is quite evident that for lower oxide thicknesses the increment in saturation current also increases.

In Fig. 13, we compare the three models by showing the drain current as a function of oxide thickness for a given supply voltage. Fig. 14, on the other hand, compares the three models by showing the drain current as function of the supply voltage for a given value of oxide thickness. Now since the Stanford and Southampton models appear to perform fairly closely with each other it is worth the while to compare them separately. Comparing the two models, as shown in Fig. 15, readily gives an indication of significant limitations due to oxide scaling, although they appear to be conformant in performance at 4 nm. The difference, however, is evident at 1 nm, where Southampton's

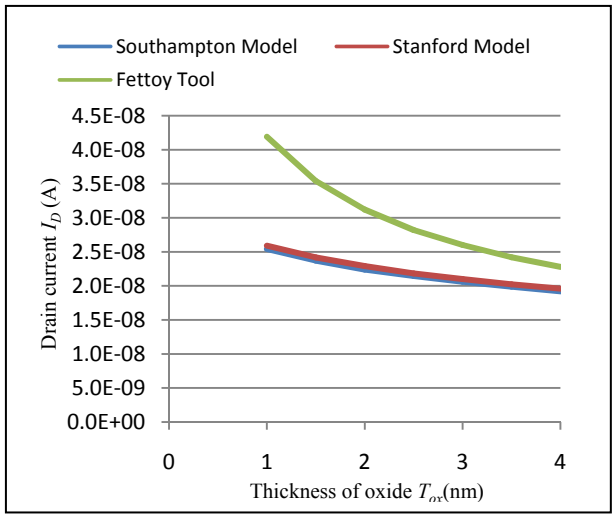

Fig. 13 Comparison between models for different thickness of oxide T_{ox} (nm).

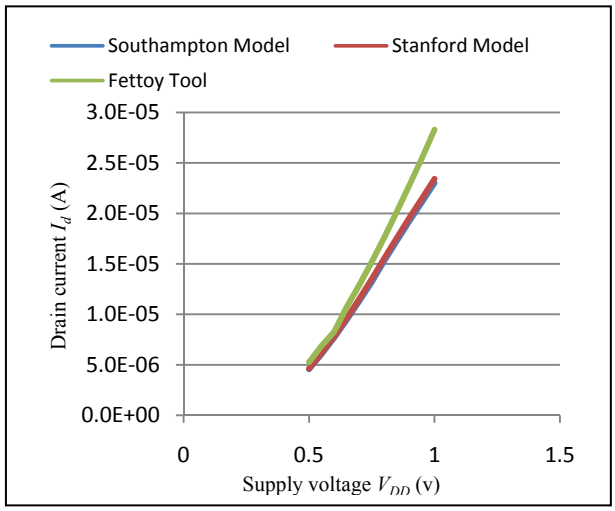

Fig. 14 Comparison between models with different values of supply voltages at T_{ox} = 4 nm.

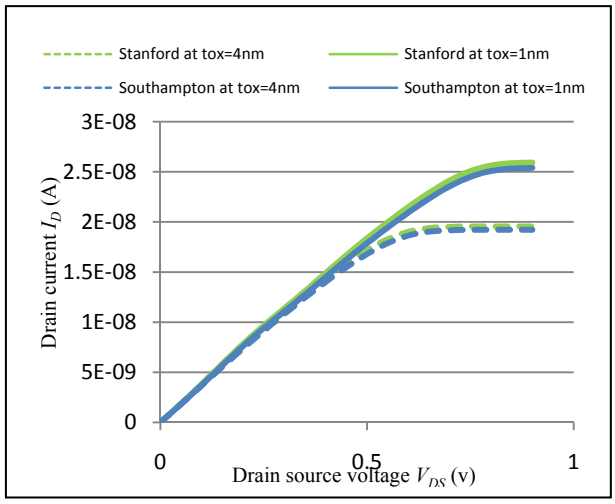

Fig. 15 Effect of oxide thickness scaling on both models at 1 nm and 4 nm for T_{ox}.

shows favorable performance since it accounts for the non-ideality in a CNTFET, so its behavior is more conformant to reality.

From Fig. 13, it is evident that the drain current of the CNTFET increases with a reduction in oxide thickness. This readily reflects on enhanced CNTFET conductivity with the conclusion that conductivity of a CNTFET is inversely proportional to the oxide thickness. Furthermore, it has been observed that reduction in oxide thickness leads to high drive current (I_{ON}) and low (I_{OFF}) which causes an increase in the I_{ON}/I_{OFF} ratio. Moreover, short channel effects which include sub-threshold swing and drain-induced barrier lowering will also be improved and are indeed close to their theoretical limits.

Similarly, supply voltage scaling is very important when evaluating models, since technology trends nowadays is to have lower supply voltages while maintaining acceptable performance; something that would reduce the power dissipation across electric circuits. As shown in Fig. 16, at 0.9 V, a higher current is evidenced, while when scaling down to 0.6 V, as in Fig. 17, an improvement in electric properties appears in the models under comparison.

Comparing the three models as shown in Fig. 18, Fettoy's tool exhibits higher current levels albeit its circuit incompatibility, where it did not account for any non-idealities. On the other hand, Roy's model in Ref. [12] is circuit-compatible but still irresponsive to changes in device parameters; something not desirable for circuits exhibiting high design complexities, which involves chips and IC's. Furthermore, this model is still not valid for all operating regions. Meanwhile, the Stanford model is a circuit-compatible model which can be used to predict dynamic and transient responses of CNTFET-based circuits which accounts for ballistic effects and takes some of the non-ballistic effects for CNTFETs into consideration.

4.1 Effects of Varying the Number of CNT's on Device Performance

In this part of the paper, we will investigate the effect

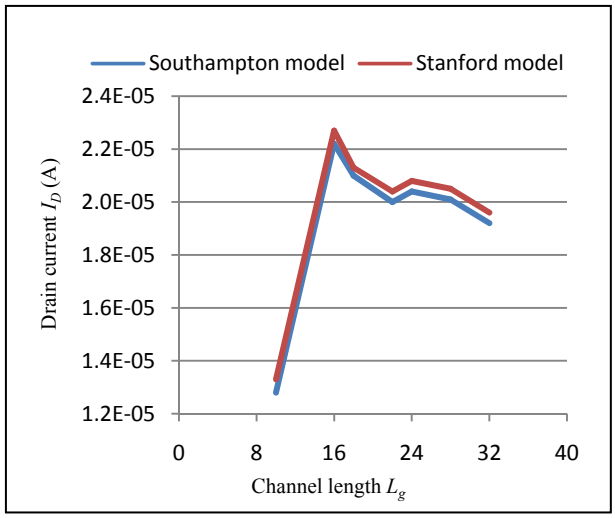

Fig. 16 Comparison of current voltage characteristics for both models at 0.9 Vsupply.

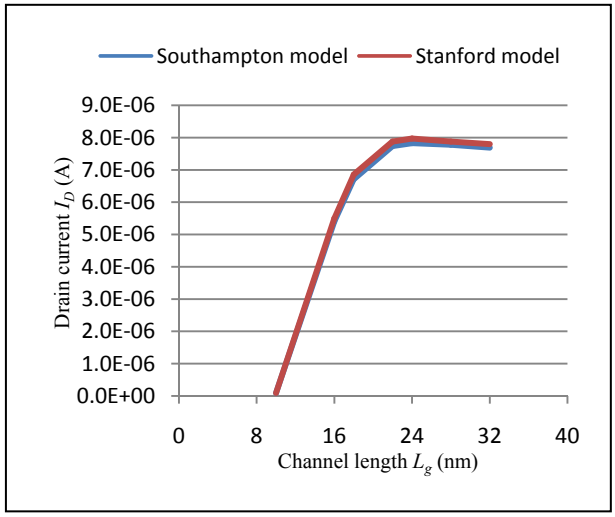

Fig. 17 Comparison of current voltage characteristics for both models at 0.6 V supply.

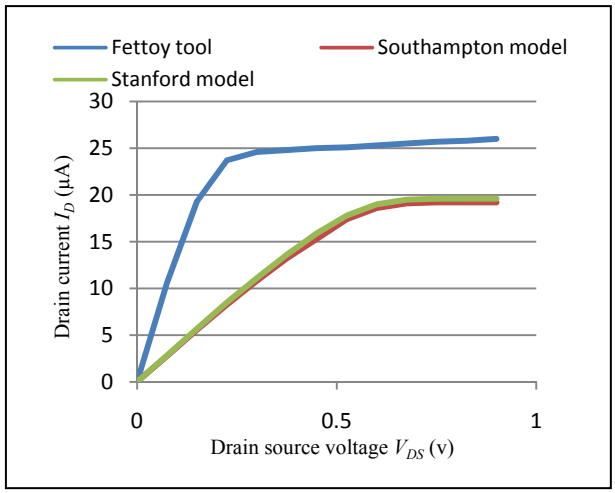

Fig. 18 Comparison of current voltage characteristics for all models.

of varying the number of nanotubes extended across the channel region of a transistor. Note that while the Southampton and Stanford models would be included in this assessment study, Fettoy's model would not. This was based on the fact that while Fettoy's model accounts for ballistic transport where the velocity is only function of energy rather than the electric field, the channel length is not accounted for. On the other hand, the Stanford model does account for quantum confinement on both circumferential and axial directions, together with acoustical/optical phonon scattering in the channel region, taking into account also the screening effects of parallel CNT's emanating from multiple CNTs, making the assessment of parallel CNTs a viable option. The Southampton model, in the meantime, is based on cubic splines with the main advantage of improving control of the approximation accuracy is also amenable for assessment under multiple CNTs.

Fig. 19 shows the Stanford model with different numbers of CNTs. Results in the figure indicate that as the number of CNTs increases the current goes up accordingly. This is shown for two values of channel length; 32 nm and 16 nm. It is clearly seen that we will have more current at 16 nm than at 32 nm.

Fig. 20 reveals similar results for Southampton's model, however, with varying levels from Stanford's. Nonetheless, when Southampton and Stanford are

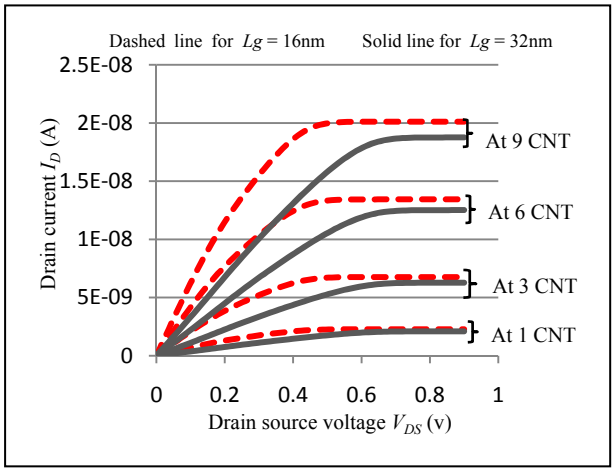

Fig. 19 Stanford model current voltage characterstics for 16 nm and 32 nm channel length at different numbers of CNT at 0.9 V supply.

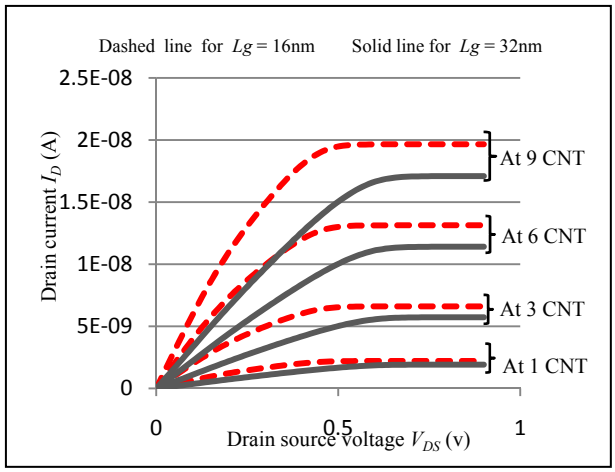

Fig. 20 Southampton model current voltage characterstics for 16 nm and 32 nm channel length at different numbers of CNT at 0.9 V supply.

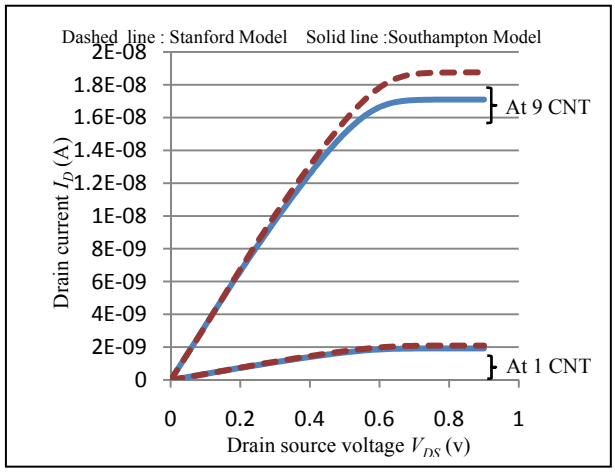

Fig. 21 Comparison for both model current voltage characterstics for 32 nm channel length at different numbers of CNT at 0.9 V supply.

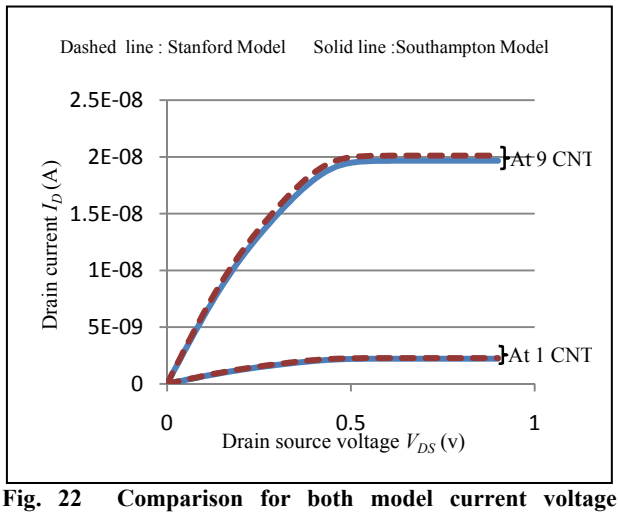

Fig. 22 Comparison for both model current voltage characterstics for 16 nm channel length at different numbers of CNT at 0.9 V supply.

compared against one another for different channel lengths, namely at 16 nm, 32 nm with the number of CNTs used as parameter, one would notice a pronounced difference between the cases of 1 CNT vs 9 CNTs. This is shown in Figs. 21 and 22.

It should be noted when considering the use of multiple nano tubes, however, that other problems may arise. This has to do with alignment of these nano tubes and the ensuing screening effect. Furthermore, scattering effects could also have some bearing.

5. Conclusions

This paper presented a comparative study between several carbon nanotube field effect transistor models assessing performance and complexity with regard to the study of scaling effects for several parameters. These parameters included channel length, oxide thickness, and supply voltage. The study evaluated each model in response to each parameter variation. It concentrated on current voltage characteristics for each model as it determines the basic parameters for a device and models its behavior in an actual circuit. The evaluation process accounted for important issues in electronics such as delay time, accuracy, and ability to develop circuits.

Under our assessment, the Southampton model was proven to be well suited for applications which require less processing time, reason being that it takes relatively little CPU (computer processing unit) time with a fair level of computational accuracy; unlike the Stanford model, which requires more CPU time with convergent accuracy comparable with that for Southampton's.

In comparison to Fettoy's, the Southampton model requires three times the CPU time, which is rather significant [14]. Also, the evaluation process accounted for important issues in electronics such as delay time, accuracy, and ability to develop circuits. Comparative evaluations are summarized in Table 1. As shown in this table the delay in Roy's model was slightly high since it depends mainly on Fettoy's that needs 11 s for evaluation [10], while it takes a larger number of

Table 1 Evaluation and comparison of models.

Models	Evaluation Parameter		
	Circuit Compatibility	Delay time	Accuracy
Fettoy tool [10]	No (Valid only for single transistor)	High (Needs 11 sec to evaluate so delay)	Insufficient
Roy model [12]	Yes	High	Good but insufficient
Stanford model [13]	Yes	Acceptable	High
Southampton model [14]	Yes	Least	High

iterations for polynomials which need more time to be evaluated correctly. According to model accuracy, it is clear that Southampton and Stanford models are more accurate than other models since both models take into account some parametric non-idealities, however, to varying degrees; things that actually happens in practical situations.

Albeit the fact that this research was devoid from any experimental data, all of the data subjects this study were extracted using HSPICE, which inherently can be a reliable source of information for a given design preceding any actual system implementation. This work was conducted under FP7, ERA-WIDE JEWEL grant no. 266507, 2010-2013; funded by the European Union.

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