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A Positive Type DVCC-Based Universal Biquad

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Abstract: This paper presents a current-mode universal biquad employing only positive type DVCCs (differential voltage current conveyors). The circuit enables LP (low-pass), BP (band-pass), HP (high-pass), BS (band-stop) and AP (all-pass) responses by the selection and addition of the input and output currents without any component matching constraints. Moreover the circuit parameters ω_0 and Q can be set orthogonally adjusting the circuit components. A design example is given together with simulation results by PSPICE.

Keywords: Analogue circuit, Biquad characteristic, DVCC, CMOS technology.

1. Introduction

High performance active circuits have received considerable attention. The circuit designs using active devices such as CCIIs (second generation current conveyors), the DVCCs, OTAs (operational trans-conductance amplifiers) and others have been reported in the literature [1-4]. A DVCC is very useful active device, and DVCC-based circuit is suitable for wide band operation. There are two kinds of DVCCs, one is positive type DVCC and another is negative type DVCC. The positive type DVCC is composed of a simpler circuit configuration than the negative type one. Hence it has a wide band operation and low power performance compared with the negative type DVCC.

The biquad is a very convenient second-order function block. Several biquads using the CCIIs, DVCCs and OTAs have been discussed previously [1-3]. However positive type DVCC-based biquad hasn't been studied sufficiently [4].

This paper focuses on a universal biquad using only the positive type DVCCs and grounded passive components as mentioned above. First we propose a basic current-mode biquad, and then show a typical current-mode circuit using the basic current-mode one. The circuit enables the LP, BP, HP, BS and AP responses by the selections and additions of the input and output currents without any component matching constraints. Moreover the circuit has an orthogonal adjusting capability for the circuit parameters ω_0 and Q.

Achievement example is given with PSPICE simulation, and the circuit workability was confirmed.

2. DVCC

The symbol of the positive type DVCC is given in Fig. 1. The DVCC is characterized by the following terminal equations:

$$V_x = V_{y1} - V_{y2}, \quad I_z = I_x \tag{1}$$

Fig. 2 shows the DVCC with MOS transistors.

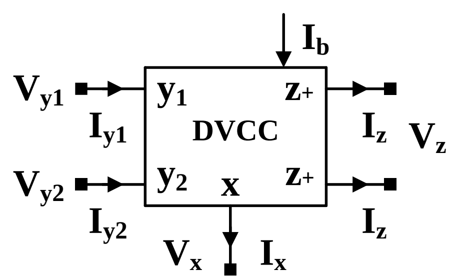

Fig. 1 Symbol of DVCC.

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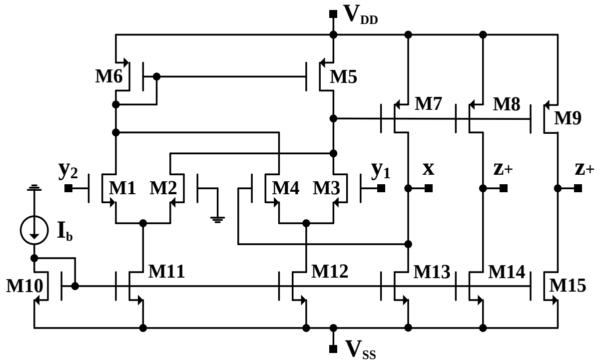


Fig. 2 Positive type DVCC with MOS transistors.

3. DVCC-Based Current-Mode Biquad

Fig. 3 shows a basic current-mode biquad configuration. This circuit is constructed with 4 positive type DVCCs and grounded passive components.

The current outputs $I_{LP}(s)$, $I_{BP}(s)$ and $I_{HP}(s)$ are given by:

$$I_{LP}(s) = -\frac{1}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1}I_i(s) \quad (2)$$

$$I_{BP}(s) = -\frac{sC_2R_1R_2/R_3}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1}I_i(s) \quad (3)$$

$$I_{HP}(s) = -\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1}I_i(s) \quad (4)$$

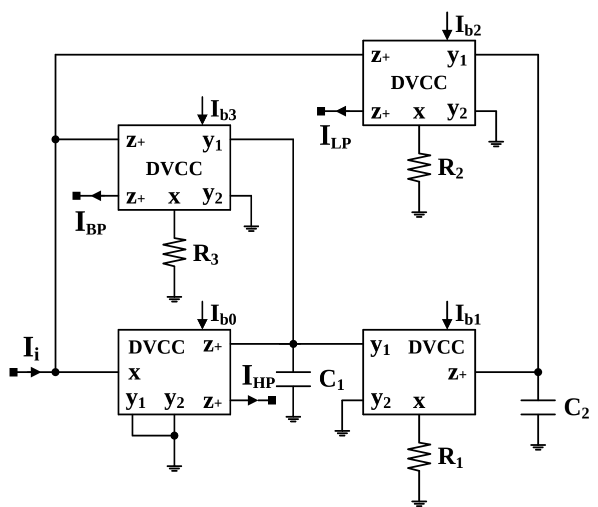


Fig. 3 Basic current-mode biquad.

The typical current-mode biquad is consisted of using the basic current-mode one shown in Fig. 4. This circuit enables the LP, BP and HP responses by selection of the output currents as follows:

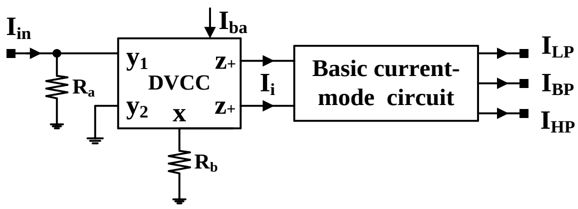


Fig. 4 Typical current-mode biquad.

$$T_{LP}(s) = \frac{I_{LP}(s)}{I_{in}(s)} = -\frac{R_a}{R_b}\frac{1}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1} \quad (5)$$

$$T_{BP}(s) = \frac{I_{BP}(s)}{I_{in}(s)} = -\frac{R_a}{R_b}\frac{sC_2R_1R_2/R_3}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1} \quad (6)$$

$$T_{HP}(s) = \frac{I_{HP}(s)}{I_{in}(s)} = -\frac{R_a}{R_b}\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1} \quad (7)$$

Moreover the BS and AP responses can be achieved by the current additions of $I_{BS}(s) = I_{HP}(s) + I_{LP}(s)$ and $I_{AP}(s) = I_i(s) + 2I_{BP}(s)$, respectively. The circuit transfer functions are given as:

$$T_{BS}(s) = \frac{I_{BS}(s)}{I_{in}(s)} = -\frac{R_a}{R_b}\frac{s^2C_1C_2R_1R_2 + 1}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1} \quad (8)$$

$$T_{AP}(s) = \frac{I_{AP}(s)}{I_{in}(s)} = \frac{R_a}{R_b}\frac{s^2C_1C_2R_1R_2 - sC_2R_1R_2/R_3 + 1}{s^2C_1C_2R_1R_2 + sC_2R_1R_2/R_3 + 1} \quad (9)$$

Thus standard circuit transfer functions can be obtained by the selections and additions of the circuit currents. The circuit parameters ω_0, Q and H are represented as below:

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_1R_2}}, \quad Q = R_3\sqrt{\frac{C_1}{C_2R_1R_2}}, \quad H = \frac{R_a}{R_b} \quad (10)$$

The circuit parameters ω_0 and Q can be set orthogonally according to the passive components, while the parameter H is able to set independently.

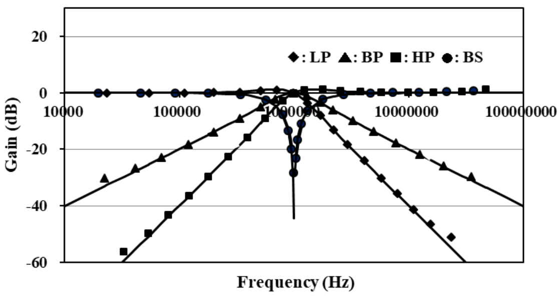
In addition, voltage-mode biquad can easily be realized using the basic current-mode one.

4. Design Example and Simulation Responses

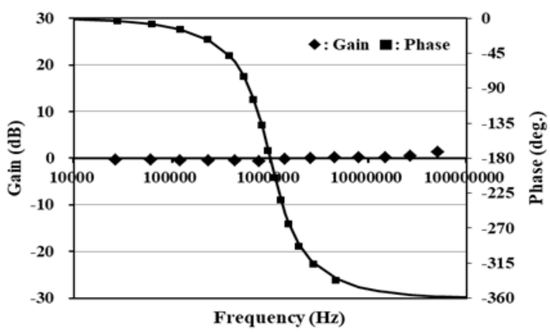
We verified the circuit operation using PSPICE simulation program. As a design example, we tried to achieve a current-mode circuit with a specification of

f_0 (= $\omega_0/2\pi$) = 1 MHz, Q = 1.0 and H = 1.0. In the simulation, we have used the DVCC shown in Fig. 2. In order to achieve the specification above, we set that the circuit resistors and capacitors were $R_1 = R_2 = R_3$ = 12 kΩ, R_a = 11.2 kΩ, R_b = 10 kΩ and $C_1 = C_2$ = 12 pF, respectively.

Fig. 5 shows the simulation responses. Fig. 5(a) shows the LP, BP, HP and BS responses, and the AP response is shown in Fig. 5(b). This can be viewed as an excellent result over a wide frequency range. Here we set that the input current, bias currents and DC supply voltages of the DVCCs were I_{in} = 10 μA, $I_{b1} = I_{b2} = I_{b3} = I_{ba}$ = 10 μA and $V_{DD} = -V_{SS}$ = 0.8 V. The power dissipation was 0.433 mW, meanwhile it was 0.450 mW in the AP response.



(a)



(b)

Fig. 5 Simulation responses.

In this simulation, we have set the aspect ratio W/L = 40 μm/0.5 μm (M1-M4), and 10 μm/1 μm (others), respectively. And we have used device parameters of MOSIS 0.5 μm for other parameters.

5. Conclusions

This paper has described a universal biquad employing only positive type DVCCs. The circuit can achieve five standard circuit responses (i.e., LP, BP, HP, BS and AP responses) by selecting and adding the input and output currents with no component matching constraints. The circuit parameters ω_0 and Q can be set orthogonally by the circuit components, and while the parameter H is set independently. The achievement example has been given together with simulation results by PSPICE. The simulation responses have been appropriate enough over a wide frequency range.

The non-idealities of the DVCC affect the circuit performances. The solution for this will be discussed in the future.

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