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IGZO/ZTO TFTs with Modulated Double Channel of Thickness Structures

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Abstract: The device characteristics of IGZO/ZTO (indium-gallium-zinc oxide/zinc-tin oxide) TFTs (thin film transistors) with modulated channels were investigated. The field effect mobility was enhanced to 20.4 cm^2/Vs in the channel-modulated TFT. The electrical performance of the TFT device was improved by the insertion of a high carrier concentration layer at the channel/gate insulator interfaces. It was due to the enhancement of carrier accumulation and the reduction of parasitic resistance via channel modulation. The threshold voltage was controlled at appropriate value. These results indicate that the device characteristic of TFTs can be enhanced by the modulated channel structure.

Key words: IGZO, ZTO, double insulating layer, double channel layer.

1. Introduction

With the rapid advancement of technology in recent years, displays have been widely used in life, from traditional CRTs (cathode ray tube) to LCDs (liquid crystal televisions), flexible screens, and smartphones. Taking the smartphones manufactured by Samsung in South Korea as an example, the panel they use is AMOLED (Active Matrix Organic Light Emitting Display) technology, and the difference from the passive structure used in the past is: active. The structure uses TFT (thin film transistor) and capacitor stored signals as an electrical conversion device to turn pixels on and off. Although the cost is more expensive and the technology is more complicated, each pixel can be driven continuously and independently. The driving signal can be memorized without the need to operate under high pulse current, the efficiency is improved, and the service life is also extended. Therefore, the TFT as the core of its operation plays a pivotal role. Due to the development of technology, people have increasingly higher requirements on the functions of the display. In order to improve the technology of the display, such as high resolution, large size, light and thin, low cost, low power consumption, etc., it is undoubtedly starting from improving the characteristics of TFTs. A good choice has also promoted the vigorous development of TFT technology.

Dual-channel TFTs with high carrier concentration sublayers at the interface of the channel and gate dielectric have shown improved device performance by increasing electron accumulation [1-4]. The performance of TFT is enhanced by Ar plasma treatment and reduction of parasitic contact resistance by inserting a layer of high carrier concentration between the channel and the electrode [5-8]. However, in these methods, there is no report on the effect of the modulation channel structure on the performance of the TFT. Therefore, in this experiment, through the RF (radio frequency) process of the IGZO (indium-gallium-zinc oxide) and ZTO (zinc-tin oxide) targets, a dual-channel TFT structure was prepared and the device characteristics were analyzed.

2. Experiment

This experiment is mainly divided into two parts: the production of TFTs and the electrical measurement

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of TFTs. The flow chart of the experiment is shown in Fig. 1. The TFT produced in this experiment has a bottom gate structure. We use a metal mask to define the shape of each layer of the TFT, and use a thermal evaporation machine to deposit aluminum 70 nm as the lower gate, and use RF magnetron sputtering (RF) yttrium oxide/alumina: 140/60 nm as the insulating layer, followed by RF magnetron sputtering to deposit the channel layer of IGZO/ZTO: 25/25, 35/15, 45/5 nm, and finally used the thermal evaporation machine deposits 70 nm aluminum as the drain and source electrodes, and the schematic diagram of the stacking of the transistor layers is shown in Fig. 2.

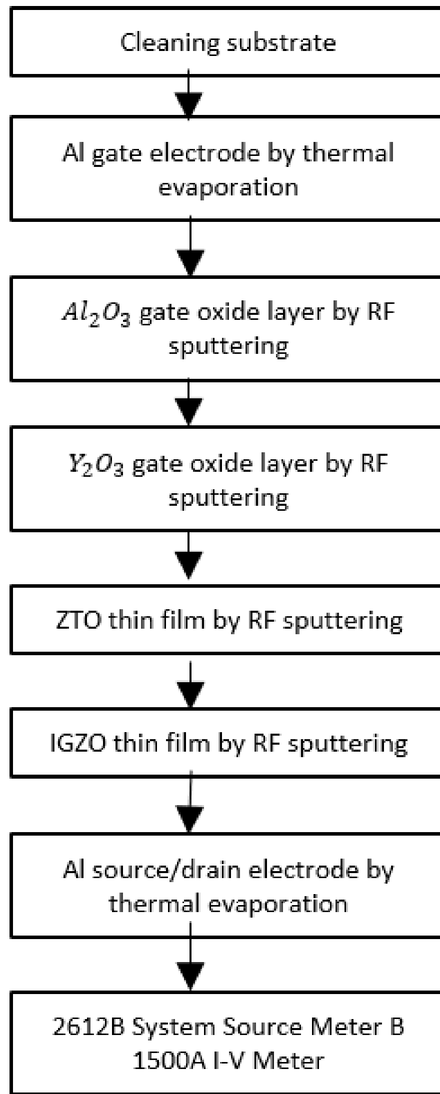

Fig. 1 Experimental flow chart.

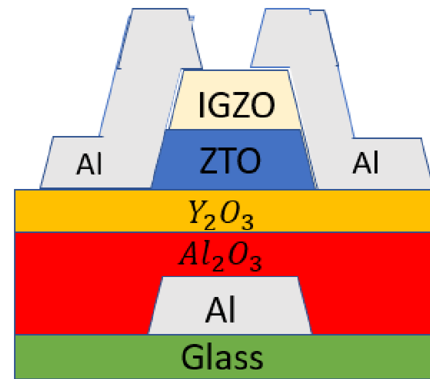

Fig. 2 Schematic diagram of IGZO TFT with IGZO, ZTO channel.

3. Results and Discussion

Fig. 2 shows the double channel TFTs consisted of a high carrier concentration layer. The detailed information of TFT fabrication process was described in the Table 1. Figs. 3a-3c show the output characteristics of a TFT with a channel layer of IGZO/ZTO. As the gate voltage increases, the current value at which the drain reaches saturation also increases. As shown in Figs. 3a-3c, the transmission characteristics of the dual channel show its excellent output characteristics. Therefore, it can be seen in Table 1 that by increasing the thickness of the ZTO layer, the transmission characteristics of the dual channel device are substantially improved. Therefore, devices under the IGZO/ZTO (25/25 nm) structure can achieve a higher mobility with a value of 20.4. According to our experimental results, TFTs with a 25 nm thick IGZO/25 nm thick ZTO double-layer channel layer have a high saturation drain current of 76.8 μA. All components are enhanced *n*-channels, because electrons are generated by positive V_{GS}, and no current crowding occurs in the output characteristics of the components, indicating good ohmic contact between the channel layer and the source/drain metal.

Figs. 4a-4c and Figs. 5a-5c show the transfer characteristics at a drain voltage of 10.1 V of the IGZO/ZTO TFTs depending on RF power of IGZO, ZTO target. When a channel was prepared by sputtering of

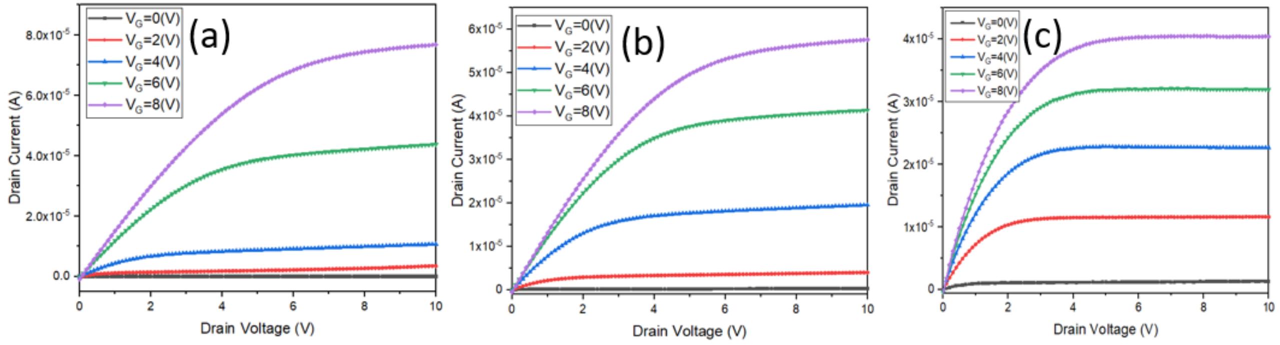

Fig. 3 Output characteristics of TFT with different IGZO/ZTO thickness: (a) 25/25, (b) 35/15, (c) 45/5 nm.

Table 1 Electrical parameters of TFTs with IGZO/ZTO channel in this work.

Y2O3+Al_2O_3-140-60 nm	V_t	SS	I_{on}/I_{off}	C_{ox}	μ_{FE}	N_t	C(nF)
IGZO+ZTO-25-25	0.85	0.11	9.7×10^4	4.815×10^{-4}	20.4	2.421×10^{15}	2.4075
IGZO+ZTO-35-15	1.45	0.13	7.5×10^4	4.815×10^{-4}	18.3	3.407×10^{15}	2.4075
IGZO+ZTO-45-5	4.25	0.15	6.1×10^4	4.815×10^{-4}	14.8	4.394×10^{15}	2.4075
IGZO+50	5.03	0.18	4.7×10^4	4.815×10^{-4}	11.7	5.991×10^{15}	2.4075

IGZO target, transfer characteristic of the TFT was not shown due to the high carrier concentration in the channel. When a channel was deposited by sputtering of ZTO and IGZO targets, the transfer characteristic of the TFT (IGZO-50) was shown. The V_t and μ_{FE} of IGZO-50 TFT were 5.03 V and 11.7 cm²/Vs, respectively. Since the carrier concentration in the oxide channel layer originates from oxygen vacancies [9, 10], the ZTO insertion suppressed the carrier concentration in the channel layer and positively shifted the V_t [11]. When the thickness of ZTO was increased to 5 nm (IGZO+ZTO-45-5), the V_t was negatively shifted to 4.25 V and the μ_{FE} was increased to 10.8 cm²/Vs. When the thickness of ZTO was increased to 15 nm (IGZO+ZTO-35-15), the V_t and μ_{FE} were 1.45 V and 18.3 cm²/Vs, respectively. When the thickness of ZTO was increased to 25 nm (IGZO+ZTO-25-25), the V_t and μ_{FE} were 0.85 V and 20.4 cm²/Vs, respectively. The V_t was negatively shifted due to the increased carrier concentration in the channel and the μ_{FE} was enhanced by the increase of the carrier concentrations. The charge density of IGZO/ZTO channels is calculated by using Eq. (1):

$$N_{ch} = C_{ox} \times \frac{V_{on}}{q \times t_c} \quad (1)$$

where C_{ox}, V_{on}, q, and t_c are the gate dielectric capacitance per area, turn-on voltage, elementary charge, and channel thickness, respectively.

Figs. 4a-4c show the transfer characteristics of the channel modulated IGZO/ZTO TFTs in logarithmic scale and Figs. 5a-5c show the transfer characteristics in linear scale to extract the threshold voltage. In order to obtain a high μ_{FE} and moderate V_t (positively positioned adjacent to 0 V), the channel modulated TFTs were fabricated. Since carrier concentrations of IGZO+ZTO-45-5, IGZO+ZTO-35-15, and IGZO+ZTO-25-25 TFTs were about the average of IGZO-50 and similar to that of IGZO+ZTO-35-15 TFT considering the deposition process, the V_t variations of IGZO+ZTO-25-25 to IGZO+ZTO-45-5 TFTs were smaller than those of IGZO-50 TFT. The channel layer of IGZO+ZTO-45-5 to IGZO+ZTO-25-25 TFT was composed of two layers, as the thickness of ZTO was increased from 5 to 25 nm during the deposition. The thickness of each layer was controlled by the deposition time. The V_t was shifted to 4.25 V and μ_{FE} was enhanced to 14.8 cm²/Vs considering IGZO+ZTO-35-15 TFT. The shift

of V_t was due to the decreased carrier concentration in the channel. The μ_{FE} was increased by the decreased contact resistance (RC), since the upper channel layer with low carrier concentration reduced the parasitic contact resistance between channel and electrode. It was reported that the RC is lower for a channel layer with a low carrier concentration. The channel layer of IGZO+ZTO-35-15 TFT was composed of two layers. The V_t shifted to 1.45 V, and the μ_{FE} increased to 18.3 cm^2/Vs. It was due to the increased carrier concentration in the channel. Since electrons accumulated mainly in the main charge conductance channel, which is located near the interface between the gate oxide and the channel layer, the TFT with a high carrier concentration layer near the gate oxide forms a current path easily and has a high μ_{FE}. The increased carrier density at the main charge conductance channel was more effective to the increase of μ_{FE} than the increased carrier density near the channel/electrode. The channel layers of IGZO+ZTO-25-25 TFT were composed of two layers. The V_t shifted to 0.85 V, and the μ_{FE} increased to 20.4 cm^2/Vs compared than IGZO+ZTO-35-15 TFT. The shift of V_t was the reduction of channel thickness with high carrier concentration in the interface between channel and gate oxide. The increase of the μ_{FE} was due to the high carrier density around the channel/gate oxide interface and the reduction of RC at the channel/electrode interfaces. The high μ_{FE} and appropriate V_t were acquired by the channel modulated TFTs; the insertion of a high carrier concentration layer at the channel/gate insulator plays an essential part in the channel formation and reduction of RC. The subthreshold swing (SS) of TFTs was in the range of 0.15-0.11 V/dec. The density of total trap states (N_t) is composed of the density of deep bulk states in the channel and the interface trap states (N_{it}) between channel and dielectric interface, it can be extracted by using Eq. (2):

$$N_t = \left[\frac{S.S.\log(e)}{kT/q} - 1\right]\frac{C_{ox}}{q} \quad (2)$$

In addition, the value of N_t was in the range from 4.394×10^{15} to 2.421×10^{15} cm^{-2}. Under this result, it can be seen that the ZTO layer can improve the gap between the double insulating layer of the gate and the oxide semiconductor channel layer. Interface performance [12] and improve the interface performance between the channel layer and the electrode, so through AFM measurement as shown in Fig. 6, IGZO/ZTO-25/25 nm surface roughness is lower than IGZO/ZTO-45/5nm. The SS value of IGZO/ZTO TFTs was relatively larger than that of previous reported papers. The decrease of density of the total trap states was explained by ZTO thickness, since ZTO affects the broadening of the gap states of the IGZO/ZTO channel layer.

Figs. 7a-7c show the hysteresis characteristics of the device displayed with positive and negative voltage scans. Table 2 shows the hysteresis of the IGZO/ZTO double-layer channel layer at 25/25 nm structure. The minimum value can be obtained as 0.254, and the hysteresis of the single-layer IGZO is low. Some hysteresis occurs when the charge is trapped at the interface between the two layers of the

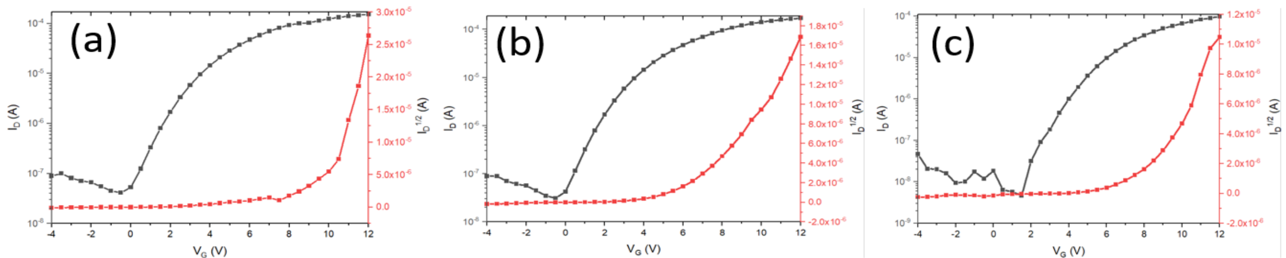

Fig. 4 Transfer characteristic of TFTs with different IGZO/ZTO thickness: (a) 25/25 nm, (b) 35/15 nm, (c) 45/5 nm.

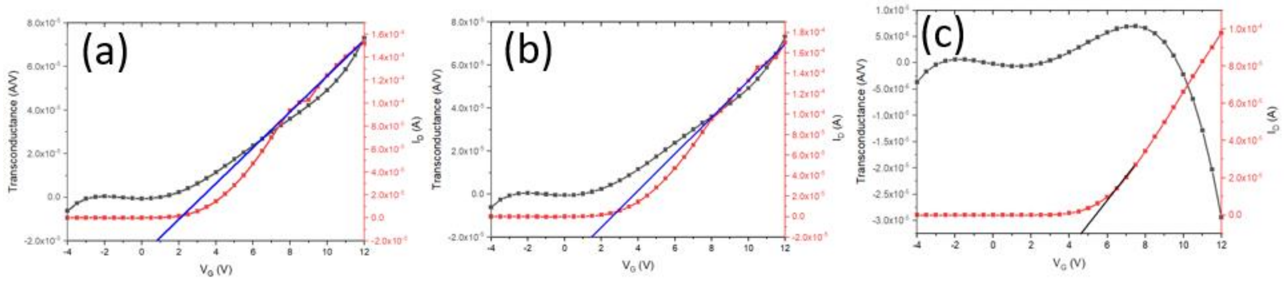

Fig. 5 Transfer characteristic of TFTs with different IGZO/ZTO thickness: (a) 25/25 nm; (b) 35/15 nm; (c) 45/5 nm.

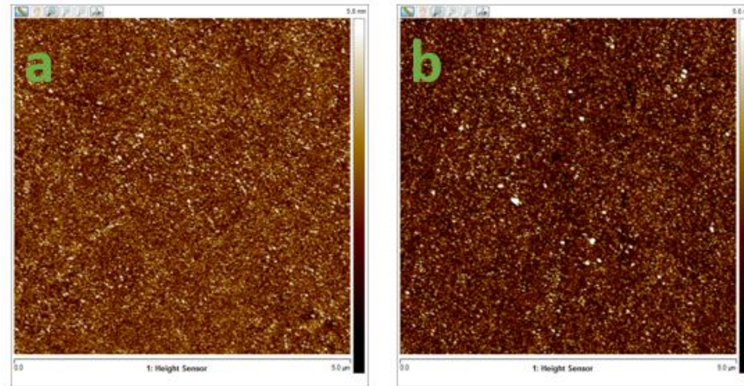

Fig. 6 AFM image of the IGZO/ZTO channel films: (a) 25/25 nm RMS (0.65), (b) 45/5 nm RMS (0.808).

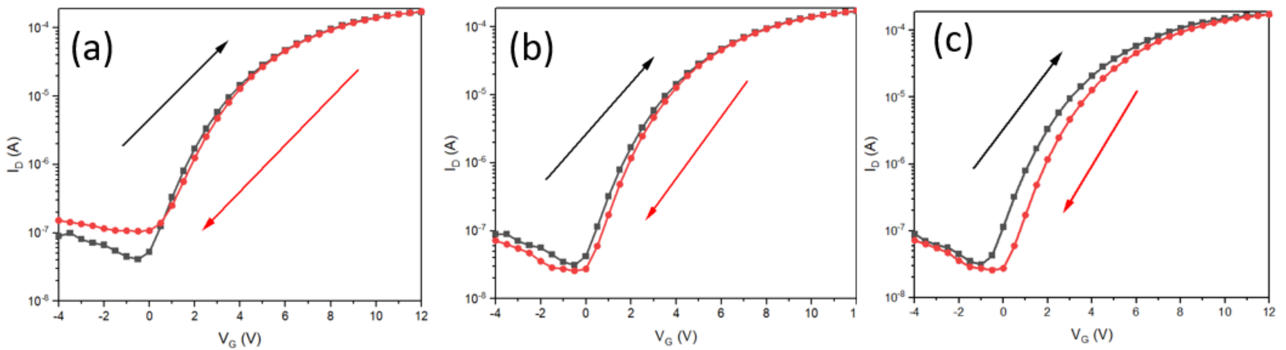

Fig. 7 Forward and reverse transfer characteristics of TFTs with IGZO/ZTO channel layer: (a) 25/25 nm, (b) 35/15 nm, (c) 45/5 nm.

Table 2 TFTs hysteresis of double-channel layer.

Y2O3+Al_2O_3-140-60 nm	Hysteresis
IGZO+ZTO-25-25	0.254
IGZO+ZTO-35-15	0.36
IGZO+ZTO-45-5	0.859
IGZO+50	0.267

gate insulating layer, and the charge trap affects the SS at the interface between the channel and the insulating layer. Therefore, it can be known that the double-layer channel can improve the interface and electrical characteristics between the insulating layer and the channel layer, so that the transistor can obtain better characteristics than the single-layer channel layer.

4. Conclusions

In this work, the best performance condition of the device is 25 nm IGZO/25 nm ZTO, which can form an

enhanced *n*-channel transistor, the hysteresis is 0.254 V, saturation current is 76.8 μA, saturation mobility is 20.4 cm^2/Vs, critical voltage is 0.85 V, I_{on}/I_{off} ratio is 9.7×10^4, SS is 0.11 V/dec, channel-insulation interface of the maximum surface energy state density is 2.421×10^{15} cm^{-2}. The insertion of a high carrier concentration layer at the channel/gate oxide affected the channel formation and enhanced the μ_{FE}. The proposed channel structure can be adopted in the TFT fabrication to acquire the high μ_{FE} and appropriate v_t. The IGZO/ZTO double-layer channel also improves the surface properties of the insulating layer, the quality of the IGZO film and reduces the interface trap density of the channel-insulating layer. This work shows that the dual-channel layer can effectively improve the transistor quality of the single-layer channel.

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