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An Active Inrush Current Limiter Based on SCR Phase Shift Control for EV Charging Systems

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Abstract: This article gives an overview of the main passive solutions and active techniques, based on AC switches to limit inrush currents in medium power AC-DC converters (up to 3.7 kW) for electric vehicle charging systems. In particular, a strategy, based on SCR (silicon controlled rectifier) phase, shift control in a mixed rectifier bridge with diodes and thyristors, is proposed. The challenge is to help designers optimize the triggering delay of SCRs to both limit the peak value of inrush current spikes and optimize the charge duration of the DC-link capacitor. A mathematical model (Mathcad engineering tool) has been defined to point out, the interest of a variable triggering delay to control SCRs to meet the expectations described previously. Experimental measurements using an industrial evaluation board of the AC-DC converter demonstrate the robustness of the method.

Key words: EV charger, AC-DC converter, inrush current limiter, SCR, phase shift control.

1. Introduction

All states that are parties to the United Nations framework convention on climate change have met annually at COP (conferences of parties) meetings since 1995. Each year, the delegates of the state parties make progress on the text which, it should be remembered, is being conducted to reveal the existence of human-induced climate change, and give industrialized countries the major part of responsibility for combating it [1]. During the 21st COP meeting, hosted and chaired by France from November 30 to December 11, 2015, EVs (electric vehicles) were a hot topic, since electric transportation must be both a critical need for the fight against climate change and a market-ready technology [2-4]. A major need consists in marketing low-cost EVs, accessible to all, including those in developing countries, with a range of 300 miles and a charging time of under 30 min [5-7]. One of the key elements in a BEV (battery EV) or a plug-in HEV (hybrid EV) is the battery charger which is responsible for charging the battery pack. Recent studies point out the importance to design a high power and high efficiency charger, while optimizing its size, charging time and the amount and cost of electricity drawn from the utility [8, 9].

One of the major issues in an EV (BEV or plug-in HEV) charger is high inrush currents generated on AC-mains, when the SMPS (switched mode power supply) is plugged in [10, 11]. Such high currents can easily be ranged from 5 times to 20 times higher than the steady state load current. Those phenomena can affect the equipment itself (such as blown fuses, tripped circuit breakers, …), lead to premature failure of individual devices (such as switches, rectifier diodes, smoothing capacitors, …) and induce an excessive current stress on AC-mains.

For medium power applications (up to 3.7 kW), AC-DC power supplies are typically composed of large bulk electrolytic capacitances (e.g., 1 μF/W for 230 V RMS (root mean square), 50 Hz AC mains), whose purpose is to smooth ripple in the rectified current prior

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being chopped at a high frequency [12]. Those capacitors are the cause of high inrush currents. At the moment, there are many passive and active solutions to limit surge current during AC-DC converters' turn-on.

This paper serves several purposes. First of all, the objective is to get a better understanding of the main passive and active inrush current limitation techniques mainly used in industrial applications. The analysis is proposed based on the following criteria: targeted application, passive or active control strategy, circuitry, and cost. Regarding active techniques, the literature review is particularly focused on AC-DC power supplies using AC switches. Then, the ultimate challenge is to highlight the relevance of an active ICL (inrush current limiter) based on the phase shift control of SCRs (silicon controlled rectifiers) used in a mixed rectifier bridge (i.e., with diodes and thyristors). Several technical tips are particularly given to both optimize the triggering delay of SCRs and achieve a cost-effective and robust design, and also taking into EMI (consideration electromagnetic interference) standards. Finally, experimental measurements are analyzed to prove the efficiency of the AC-DC converter that implements the ICL described above.

2. Review of the Background and Motivations

At the moment, the common charger that is used in EV includes an AC-DC converter with PFC (power factor correction) to achieve high efficiency and meet regulatory standards for AC mains. Three AC-DC topologies are typically used: conventional boost converter, bridgeless PFC boost converter and interleaved PFC boost converter [13].

This section of the manuscript focuses on the main passive and active methods used to limit inrush currents. Also, to simplify the study and improve the readability of all electrical schematics, we consider that, the AC-DC converter implements a PFC-SMPS.

The literature review is based on the following articles [14-18] and US patents [19-23].

2.1 Main Passive Inrush Limiting Techniques

As can be seen in Fig. 1, the first passive solution to limit inrush current consists in using a large oversized inductor depending on the load. As widely reported in literature [14-16], the inductance can reach 1 H depending on the application. This strategy can be limited by the physical properties of the inductor (i.e., saturation of the magnetic core). Moreover, today's power supplies must be as compact as possible. Hence, this technique is not viable anymore.

Most of the ICL use a variable resistance such as a NTC (negative temperature coefficient) thermistor (Fig. 2a). In that case, the operation principle of this solution is quite simple. When the current flow increases inside the application, the temperature of the thermistor increases and its resistance decreases allowing nominal steady state current to flow. The main drawback of this solution is clearly that, it is necessary to let the thermistor cool down (recovery time) to reset it to high resistive mode. The cooling period can be achieved through a mechanical relay connected across the NTC thermistor. It is important to note that, the use of an electromechanical relay has several drawbacks: bulky solution, high current consumption of the coil, risk of relay opening in case of vibrations, risk of explosion in flammable environment. An AC switch (i.e., SCRs) can replace the electromechanical relay to solve those problems.

Another solution consists in connecting a NTC thermistor in series with the AC line (Fig. 2b). This NTC thermistor is coupled with a bypass switch (i.e., electromechanical relay or an AC switch such as a Triac (triode for alternating current).

The main drawback of the solutions presented in Fig. 2 is that, the NTC thermistor induces an impedance which is always connected to the AC line (through the rectifier bridge) even if the application is in stand-by mode. A switch can be added in series with the AC line before the bypass device (i.e., NTC thermistor coupled with an electromechanical relay or an AC switch) to avoid this problem. Indeed, this switch is used to

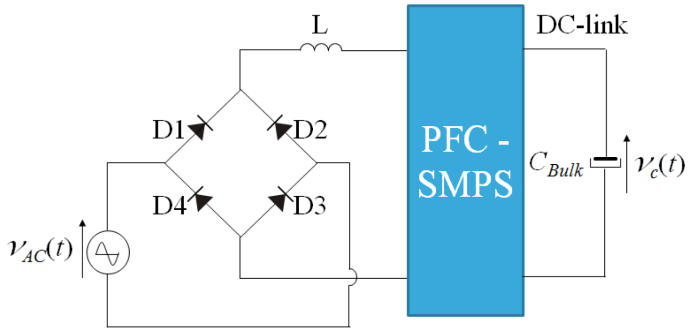

Fig. 1 ICL using an inductance.

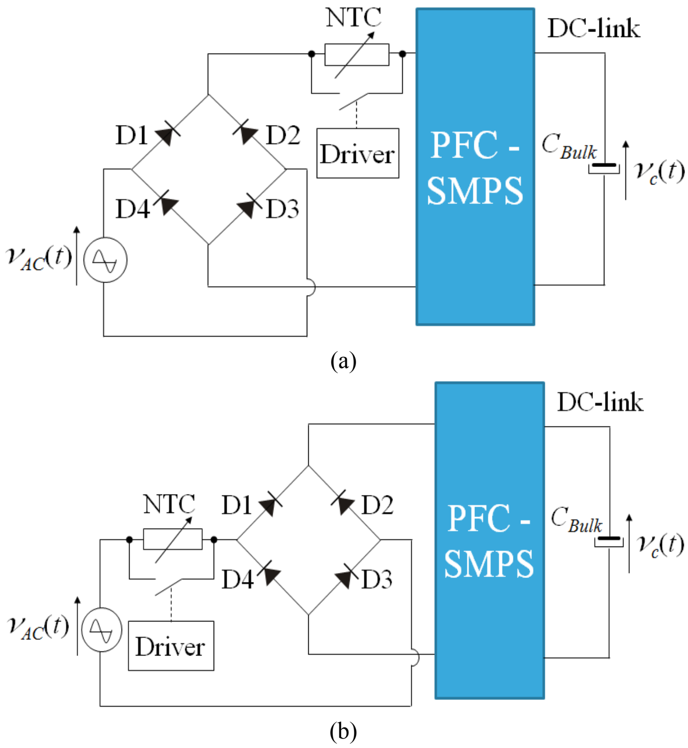

Fig. 2 ICL using NTC thermistors coupled with a relay or an AC switch.

disconnect the rectifier bridge in stand-by mode. As a consequence, the stand-by losses can be minimized.

A smarter solution consists in removing the NTC thermistor.

2.2 Main Active Inrush Limiting Techniques Based on AC Switches

It is possible to propose inrush current limitation techniques using active semiconductor devices. In this article, we focus on solutions that embed AC switches (SCRs or Triac).

Two active solutions can be studied. The first one consists in placing a thyristor in series with the DC bus (Fig. 3). The second one uses a Triac connected in series with the AC mains (Fig. 4). It is important to note that, this latter solution is only available for low power applications, today. Regarding Fig. 4, it could be interesting to use a low-loss AC switch to decrease the losses and increase the efficiency of the AC-DC converter [17].

The limitation of inrush currents is done by controlling the phase shift of the power switch. One important drawback of this solution is that, the energy efficiency of the converter is mainly affected due to the

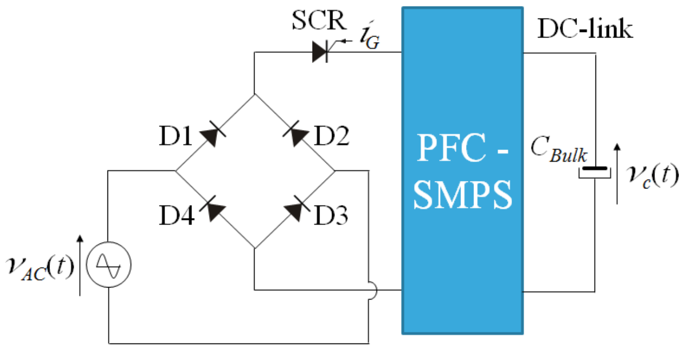

Fig. 3 ICL using a thyristor in series with the DC bus.

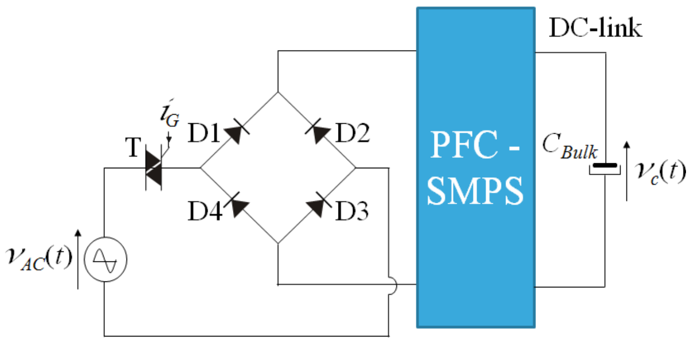

Fig. 4 ICL using a Triac in series with the AC mains.

diodes in the rectifier bridge. Therefore, there is a compromise between the cost-effectiveness and the robustness of the ICL solution. It is important to note that, phase shift controllable switch can be used in the rectifier bridge to address the objectives defined previously. This technique is presented in the next section of this article.

2.3 Active ICL Proposal Based on SCR Triggering Delay Control

Inrush currents are typically limited by the DC-link capacitance, named bulk capacitance (C_{Bulk}) in this manuscript. As can be seen in Fig. 5, this issue can be solved using SCRs to replace the high side diodes of the rectifier bridge.

In this document, the ultimate challenge is to help designers optimize the phase shift angle of each SCR (see the topology presented in Fig. 5) to both limit peak inrush currents and optimize the charge of the bulk capacitance. In particular, the aim is to give some tips to build the control algorithm of each SCR that will be implemented in the MCU (microcontroller) to meet the expectations described above.

The control circuit of each SCR induces a triggering

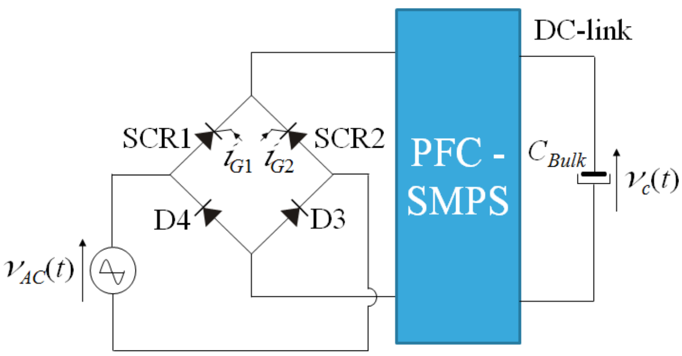

Fig. 5 ICL using SCRs.

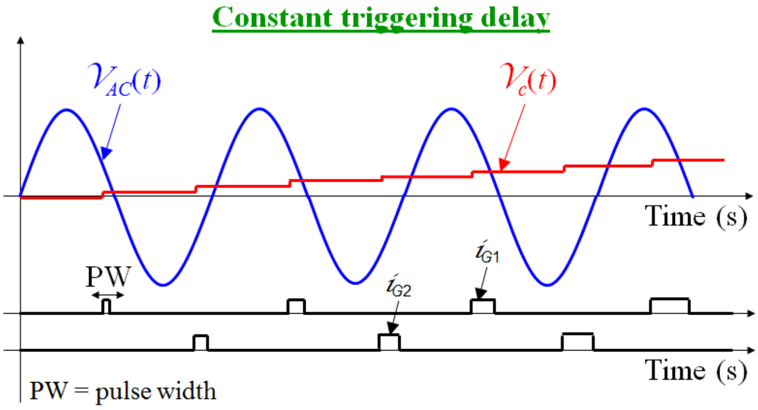

Fig. 6 SCR phase shift control principle using a constant triggering delay.

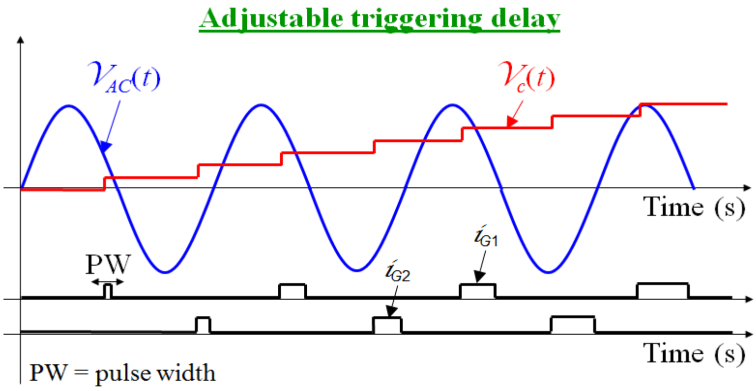

Fig. 7 SCR phase shift control principle using an adjustable triggering delay.

delay (Δt). There are also two possibilities: a constant Δt-value and an adjustable one. For each case, the gate current PW (pulse width) is incremented at each SCR turn-on, depending on the Δt-value.

Regarding the constant Δt-value control strategy (Fig. 6), it is important to note that, the duration to charge the bulk capacitance of the AC-DC converter can be too important (about 1 s). Conversely, Fig. 7 exhibits that, the bulk capacitance charge duration can be decreased (the typical value of the charge is about 100 ms) using an adjustable Δt-value.

Such a comparison between the two control strategies (constant or adjustable triggering delay of the SCRs) can only be performed if the current level is the same.

3. Methodology Used to Model Inrush Currents

3.1 General Purpose

Fig. 8 shows the topology of the AC-DC converter we want to model. In this kind of structure, a conventional PFC boost stage can be used. A bypass diode (D_{Bypass}) is responsible for charging the bulk capacitor (C_{Bulk}) before the PFC-SMPS operates.

An input filter is typically put on the AC side to address EMI requirements. This input filter is composed of several L-C stages. These elements lead to an impedance that cannot be neglected. The capacitance (about 100 nF) of one L-C stage is lower than the inductance. Consequently, the capacitor can be removed to simplify the modeling of the input filter. Finally, it is important to measure the impedance of inductor and implement the values in the mathematical calculations. It is also important to take into considerations the equivalent circuit of the AC mains and bulk capacitance to warrant the modeling accuracy.

The aim of this study is to both control the inrush current phase and the charge of the bulk capacitance during the AC-DC power supply startup. To achieve

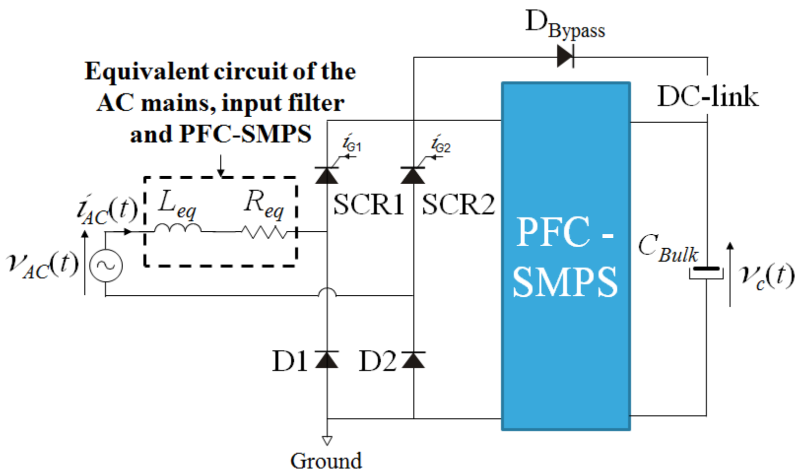

Fig. 8 Electrical schematic of the AC-DC power supply to be modeled.

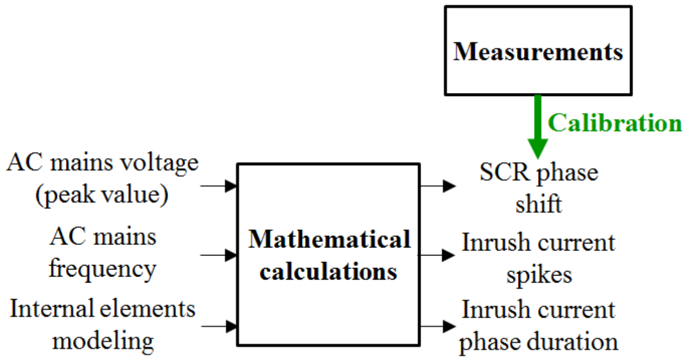

Fig. 9 Methodology used to model inrush currents.

this goal, we propose to use an engineering calculation tool (for example, Mathcad) to characterize the start-up phase, i.e., current spikes, start duration (Fig. 9). The input data are the frequency and the RMS voltage of the AC mains, as well as the equivalent components of the input filter (inductances and resistances), SCR and diode (dynamic resistances) during each half line cycle. The key element of this calculation sheet is the phase-shift control of each SCR. It is important to note that, this control strategy depends on the triggering delay (Δt) as described in the previous section. Among other things, the accuracy of this mathematical modeling depends on the parasitic elements of the input filter. First of all, it could be interesting to estimate their values according to experimental measurements (impedance meter) and then, use those values in the calculation sheet.

Of course, mathematical simulation results are calibrated with many experimental measurements.

3.2 Engineering Calculations

3.2.1 Foundations of the Mathematical Modeling

According to Fig. 8, when the SCRs are controlled, an alternating current ($i_{AC}(t)$) is flowing through the input filter. The aim is to charge the bulk capacitor before the SMPS operates. The variation of the voltage across the bulk capacitor ($v_C(t)$) is defined in Eq. (1). This equation takes into consideration the modeling of the AC mains (equivalent inductance and resistance), input filter (common mode inductance and resistance), bulk capacitance (equivalent serial resistance) and dynamic resistances of the SCRs and diodes.

$$L_{eq} C_{Bulk} \frac{\mathrm{d}^2 v_C(t)}{\mathrm{d}t^2} + \left(R_{eq} + R_{SCR} + R_{Diode}\right) C_{Bulk} \frac{\mathrm{d}v_C(t)}{\mathrm{d}t} + v_C(t) = v_e(t) \tag{1}$$

where, $L_{eq} = L_{input\,filter} + L_{AC\,mains}$, $R_{eq} = R_{AC\,mains} + R_{input\,filter}$ + ESR, ESR = equivalent serial resistance of the bulk capacitor.

The mathematical sheet solves the differential equation described in Eq. (1). Thus, it is possible to determine $v_C(t)$. From this result, the evolution of the current through the bulk capacitance can easily be calculated from Eq. (2). It is important to note that, the value of this current is calculated at any time of the SCR triggering.

$$i_C(t) = C_{Bulk}\frac{\mathrm{d}v_C(t)}{\mathrm{d}t} \quad (2)$$

Two cases must be distinguished depending on the Δt-parameter that is fixed by the application requirements, i.e., constant value or adjustable value.

3.2.2 SCR Control with a Constant Triggering Delay

Fig. 10 gives the algorithm used to control each SCR of the mixed rectifier bridge with a constant triggering delay. This control strategy is implemented in the engineering calculation tool (Mathcad).

The aim of the method is to determine the peak value of the inrush current flowing through the AC line ($i_{AC}(t)$) at each SCR triggering delay. The procedure is repeated until the bulk capacitance is fully charged, i.e., the voltage across it ($v_c(t)$) reaches its steady-state (i.e., the peak value of the mains voltage).

Using this method, the charge of the bulk capacitance lasts approximately 1 s. This could be too much long and especially if designers want to adapt this method to any other industrial needs such as lighting applications.

Therefore, a challenge consists in developing a new technique based on an adjustable triggering delay of each SCR.

3.2.3 SCR Control with an Adjustable Triggering Delay

Fig. 11 gives the algorithm used to control each SCR of the mixed rectifier bridge with an adjustable triggering delay. This control strategy is implemented in the engineering calculation tool (Mathcad) too.

Contrary to the solution described previously, the method consists in helping designers to calculate the phase shift of the SCR to have a constant peak value of

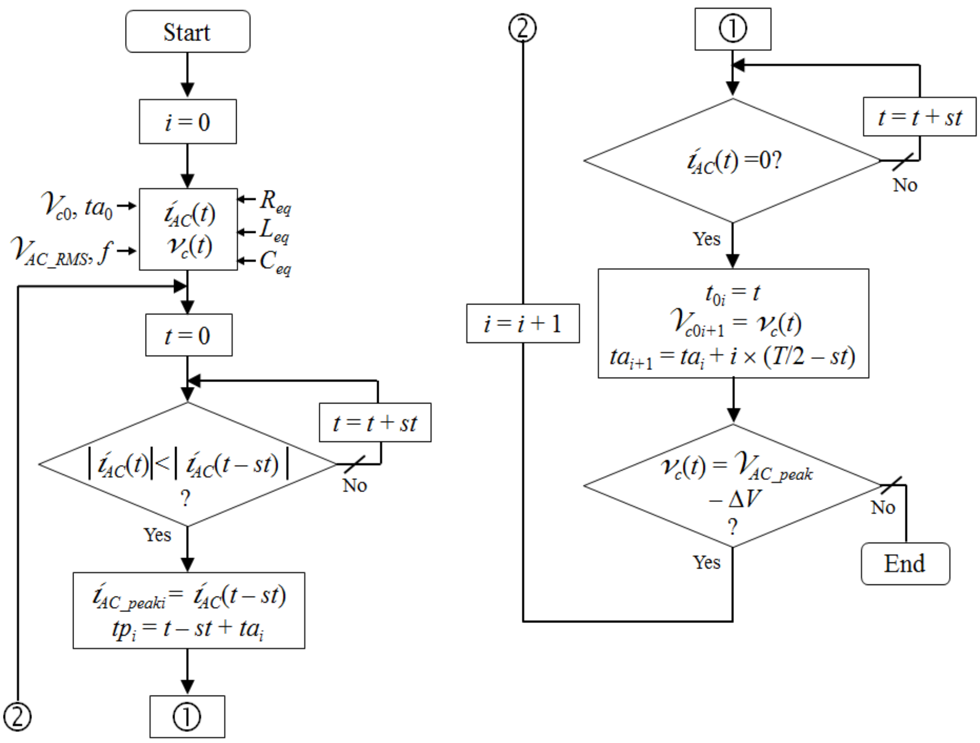

Fig. 10 SCR control algorithm with a constant triggering delay.

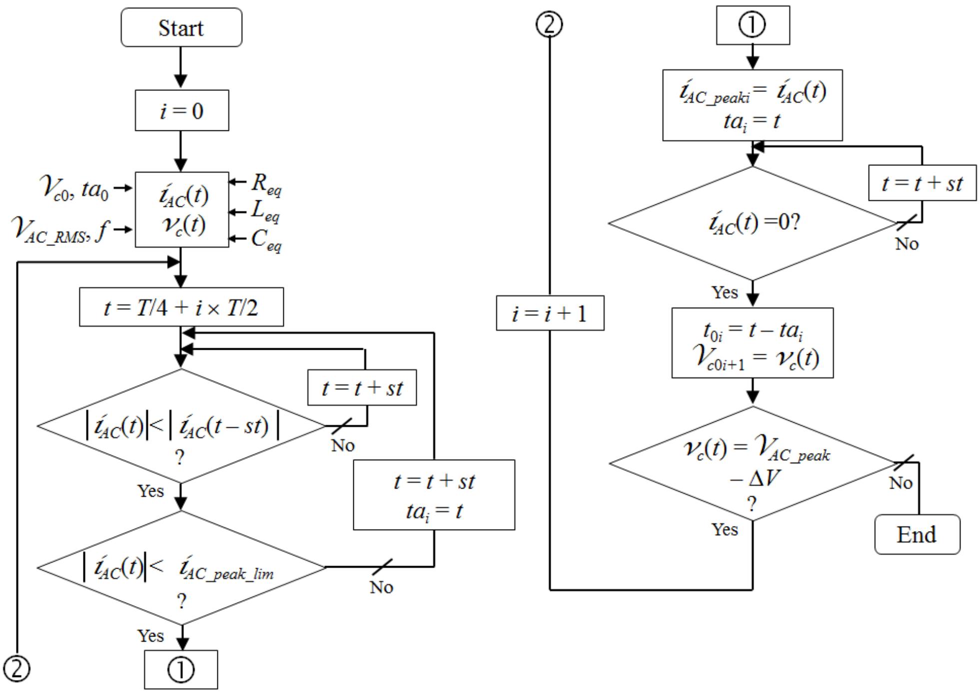

Fig. 11 SCR control algorithm with an adjustable triggering delay.

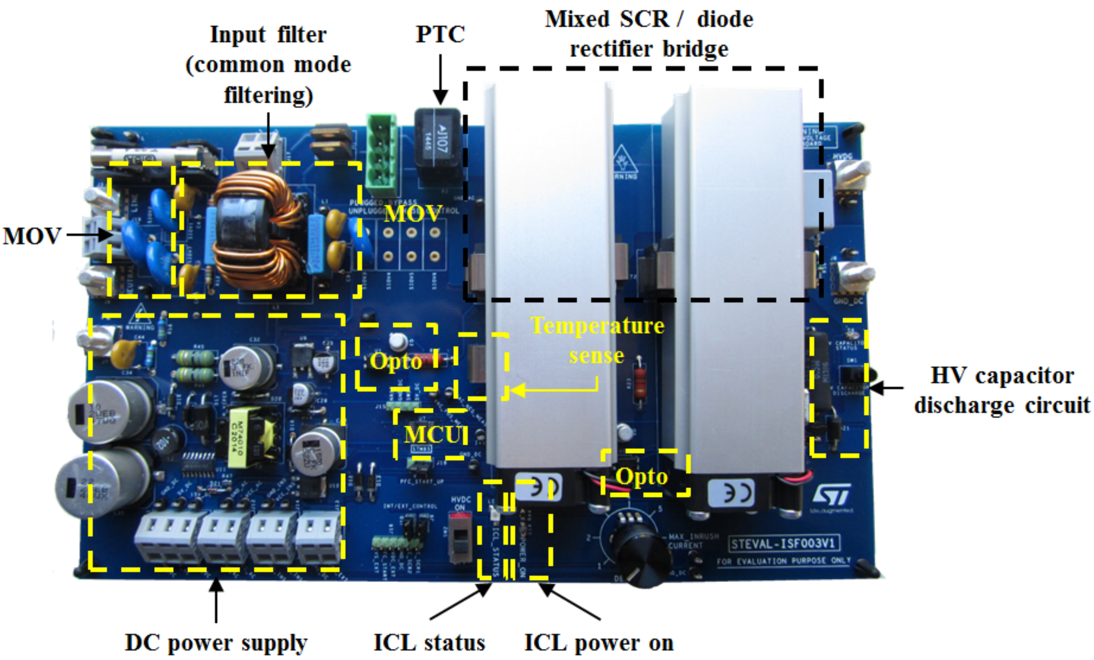

Fig. 12 STEVAL-ISF003V1 evaluation board presentation (top view).

the current flowing through the AC line. Using this technique, the charge of the bulk capacitor is faster.

4. Experimental Validation and Discussion

4.1 Evaluation Board Presentation

A board (Fig. 12) has been designed to evaluate the robustness of the AC-DC converter that embeds the ICL described above.

When the board is started, the inrush current limitation is based on a soft-start procedure to gradually control the phase-angle of the SCRs in a mixed rectifier bridge (i.e., with diodes and SCRs).

Using this strategy, it is possible to limit inrush currents, especially to be compliant with the IEC 61000-3-3 standard, since it is part of EMC (electromagnetic compatibility) trends and concerns in current and future BEVs and plug-in HEVs. It is important to note that, the IEC 61000-3-3 standard gives the limitation of voltage changes and fluctuations for equipment with rated RMS current lower than 16 A. Those fluctuations can be generated by the equipment itself in case of a too high current sunk from the AC mains. So, a voltage drop can be created due to the impedance of the AC line.

The evaluation board also allows the standby losses to be drastically reduced as the DC bus can be totally disconnected from the AC mains when it does not have to operate. The DC bus turn-off is achieved by turning-off the SCRs in the mixed rectifier bridge.

4.2 Experimental Validation of SCR Control with a Constant Triggering Delay

Fig. 13 shows the evolution of the voltage across the bulk capacitance (1 mF, 230 V RMS, 50 Hz AC mains) when the control of SCR is performed using a constant triggering delay (i.e., 50 µs). In particular, a comparison between the experimental measurements and engineering calculations (Mathcad) is proposed.

From the measurements and calculations, the charge of the bulk capacitance lasts 814 ms and 900 ms, respectively. The error rate (in comparison with measurements) is about 10%. This error rate can be decreased by adjusting the initial value of the voltage across the bulk capacitance. In the mathematical sheet, it is important to note that, this value depends on the voltage drop across each equivalent element of the AC-DC converter (i.e., AC mains, input filter, bulk capacitance, dynamic resistance of each semiconductor device).

Regarding the absorbed input current evolution (Fig. 13), the experimental measurements exhibit that, the current spikes can be higher than 9.6 A (resp. -9.6 A). The difference between the experiments and calculations may be due to the approximation of the grid impedance. So, it could be interesting to characterize the grid impedance (R-L-C circuit) using a network analyzer coupled with an attenuator. Then, the modeling results may be used in the engineering calculation sheet.

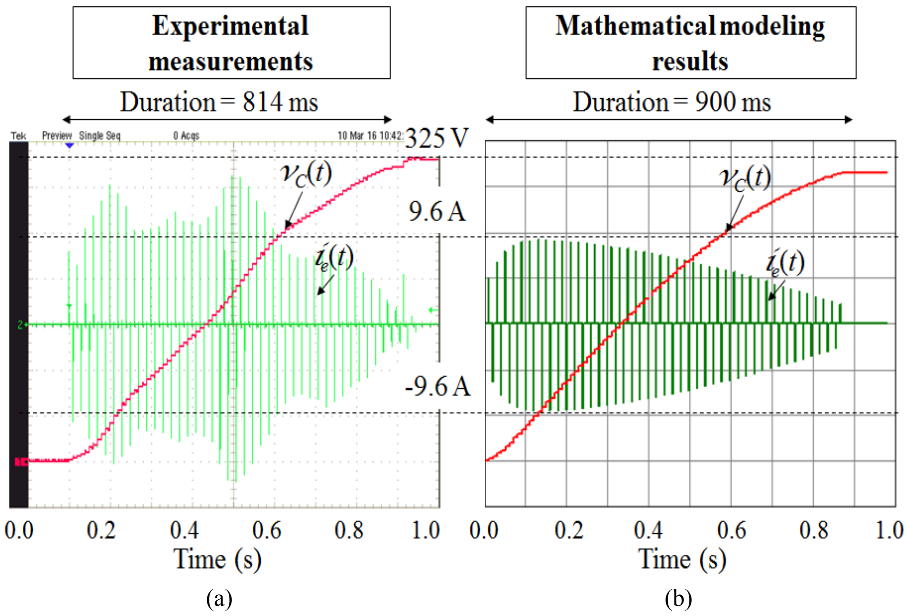

Fig. 13 Experimental measurements and engineering calculation (Mathcad) results comparison of the voltage across the bulk capacitance (1 mF, 230 V RMS—50 Hz AC mains), and absorbed input current for a constant SCR triggering delay (50 µs).

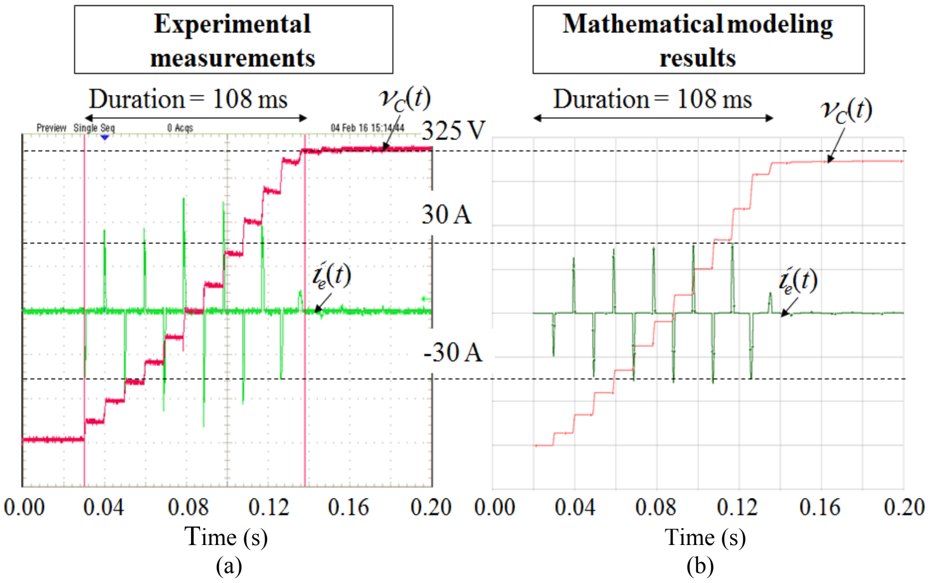

Fig. 14 Experimental measurements and engineering calculation (Mathcad) results comparison of the voltage across the bulk capacitance (1 mF, 230 V RMS—50 Hz AC mains) and absorbed input current for an adjustable SCR triggering delay.

4.3 Experimental Validation of SCR Control with a Variable Triggering Delay

Fig. 14 shows the evolution of the voltage across the bulk capacitance (1 mF, 230 V RMS, 50 Hz AC mains) in case of a soft start when the control of SCR is performed using an adjustable triggering delay. As previously, a comparison between the experimental measurements and engineering calculations (Mathcad) is proposed.

The measurements and calculations show that, the charge of the bulk capacitor lasts the same duration (108 ms). Therefore, using the adjustable Δt-value to control the SCRs, the engineering calculations give approximately the same results as experiments. However, it is important to note that, the capacitor of the DC bus is not fully charged with the constant input current spikes whatever the case (experiments and engineering calculations). We remind that, the voltage across this capacitance will reach its steady-state in the next commutation of the SCR, i.e., at a duration equal to the sum of the previous value of phase shift and a half period of the AC mains (e.g., 10 ms for 50 Hz AC mains).

Regarding the absorbed input current evolution (Fig. 14), the experimental measurements exhibit that, the current spikes can be higher than 30 A (resp. -30 A) for the same reasons as those explained in the previous section of the document.

5. Conclusions

This paper consists in proposing an efficient and low-cost active inrush current limiter that is embedded in AC-DC power supplies dedicated to electric vehicle charging systems. The circuitry is based on the control of the triggering delay of thyristors. Two control methods have been studied. In particular, the charge of the DC-link capacitor can be reduced and the AC input current spikes can be reduced using the thyristors' control strategy based on an adjustable triggering delay.

This article gives also some tips to help designers choose the best value of the triggering delay to both limit the charge duration of the DC-bus capacitor and inrush currents. Those methods have been modeled using an engineering calculation tool (Mathcad). The experimental measurements demonstrate the robustness of the modeling.

The smart control of SCR to limit inrush currents may be used in any type of AC-DC power, supply topology for electric vehicle chargers on one hand, can and be used in other applications such as servers or lighting applications on the other hand.

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